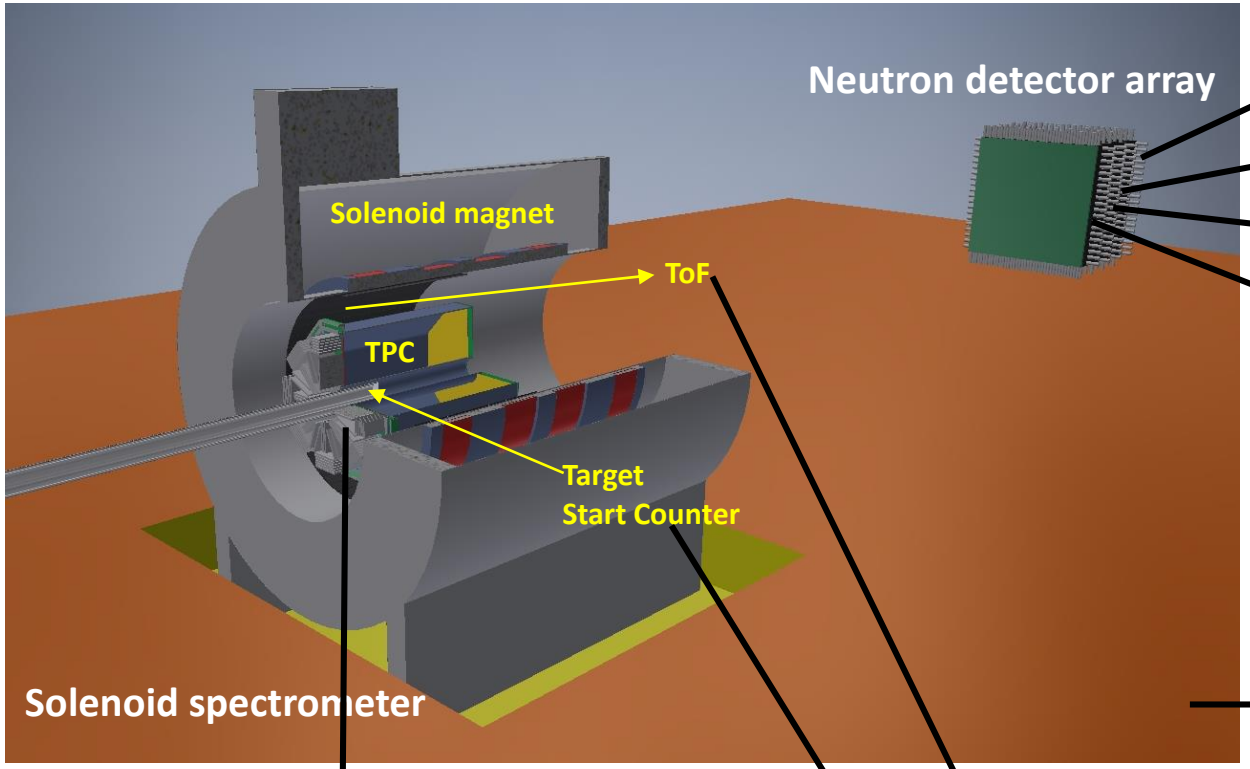
Current status of LAMPS DAQ system

HyoSang Lee

2019.04.04

Conceptual design of LAMPS DAQ system



FADC0 TCB0
FADC1 TCB1
FADC2 TCB2
FADC3 TCB3

nDAQ PC0
nDAQ PC1
nDAQ PC2
nDAQ PC3

signal
usb
UTP
10G optical

Time stamp sync.

LAMPS Trigger Electronics 2

1G/10G switch

Time stamp sync.

Slow control & monitoring system

1G switch

CoBo – uTCA2
CoBo – uTCA1
CoBo – uTCA0

Start Counter & ToF DAQ system

LAMPS Trigger Electronics 1

Gate & trigger signal

Control

TPC Data

Narval DAQ PC

1G/10G switch

Control room

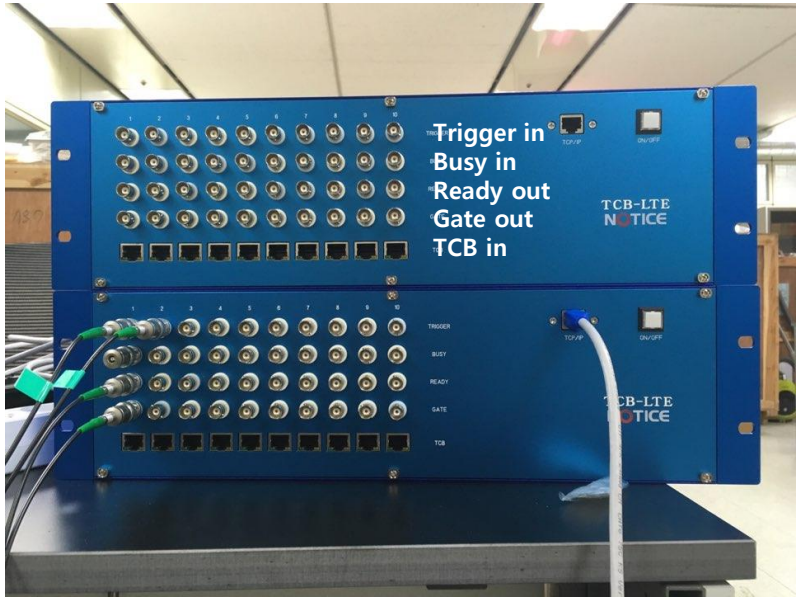
Control DAQ PC

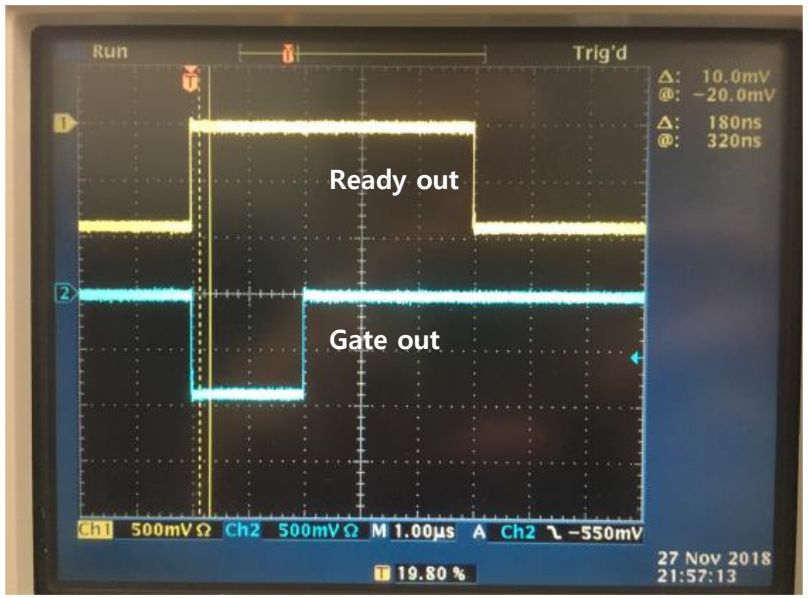
Slow control PC

Storage server pc farm
NFS system

Monitoring PC

LAMPS Trigger Electronics (LTE)





- Input : 10ch NIM/TTL + 10ch TCB (from FADC system) + Busy
- Output : trigger ready + gate

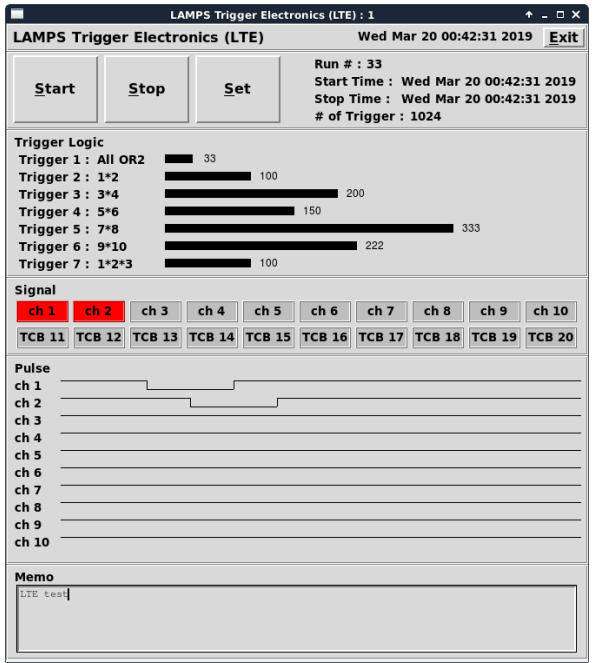
- 125Mbps LVDS serial communication

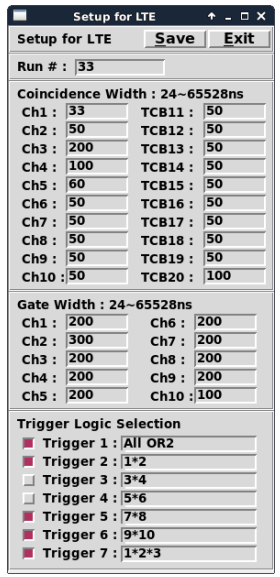
- Programmable trigger logic
  - Maximum 7 trigger logic
  - Multiplicity logic

- Event (time) synchronized between two LTEs
- Time synchronized with TCB of FADC DAQ

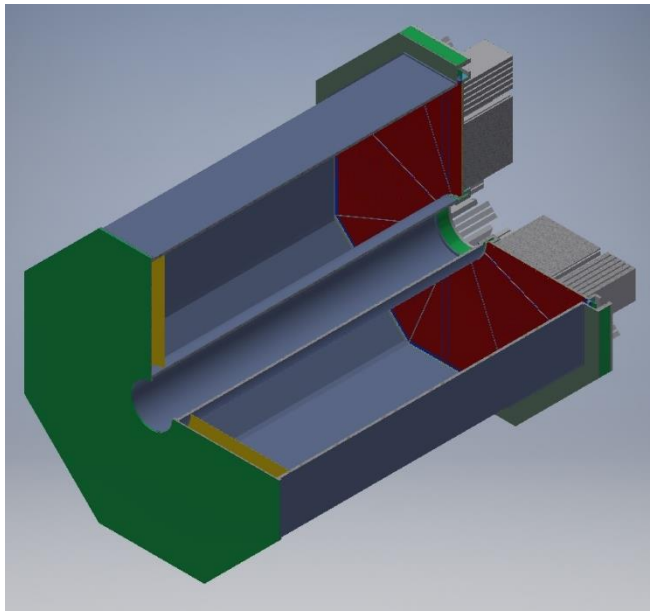
- Save all trigger information
  ch : scaler : trigger # : trigger time : trigger pattern : gate flag

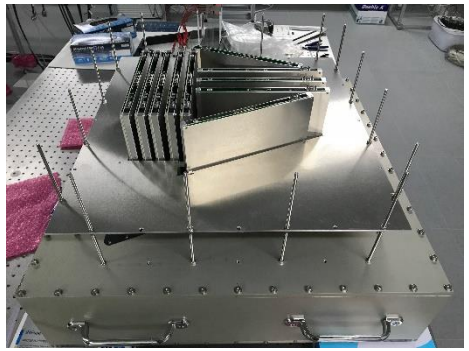
LTE control & monitoring program : c++ & perl/tk





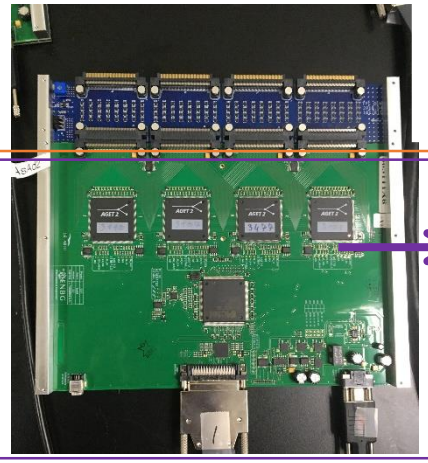
GET system for TPC

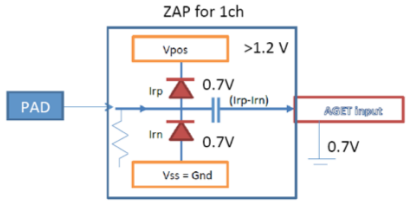




All systems are ready.
ZAP board : 120ea
AsAd board : 120ea
CoBo : 30ea
Mutant : 3ea
micro-TCA : 3ea

TPC PAD → ZAP → ASAD → COBO Mutant → DAQ PC





ZAP board
- ✓ To protect AGET chip in AsAd board
- ✓ BAV99 chip
- ✓ Made in RISP

A(Asic)GET chip

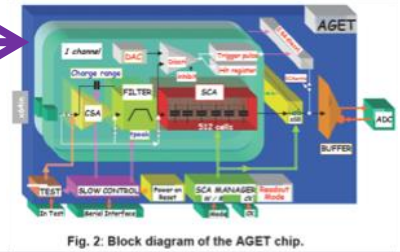


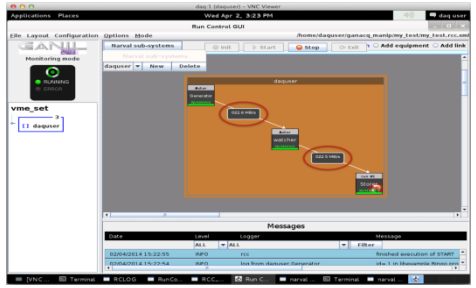
Fig. 2: Block diagram of the AGET chip.

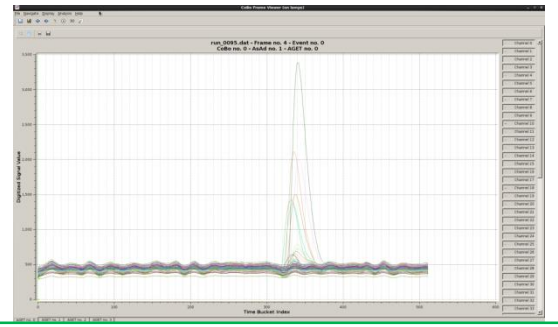
AsAd : AGET Support for Analog to Digital
- ✓ 4 AGET (256 ch) in 1 AsAd
- ✓12 bit ADC

COBO : COncentration BOard
- ✓Digital data from ASAD
- ✓Zero suppression
- ✓Network transfer to PC
- ✓4 ASAD controlled by 1 COBO

Mutant : MUtiplicity, Trigger ANd Time
- ✓3 trigger level
- ✓L0 : external trigger
- ✓L1 : multiplicity trigger
- ✓L2 : hit pattern trigger

Narval DAQ

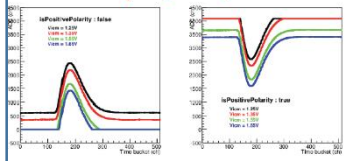




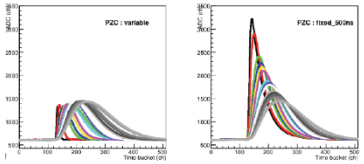
GET system test & test with GET system

Specification of GET system

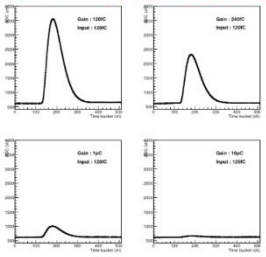
Polarity - negative or positive



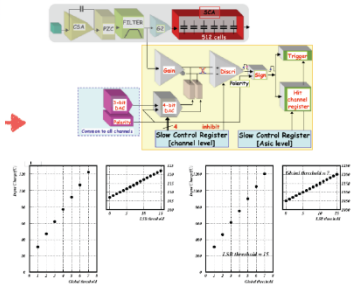
Peaking time - 50s to 1us (16 values)



Dynamic range - 120fC, 240fC, 1pC, 10pC

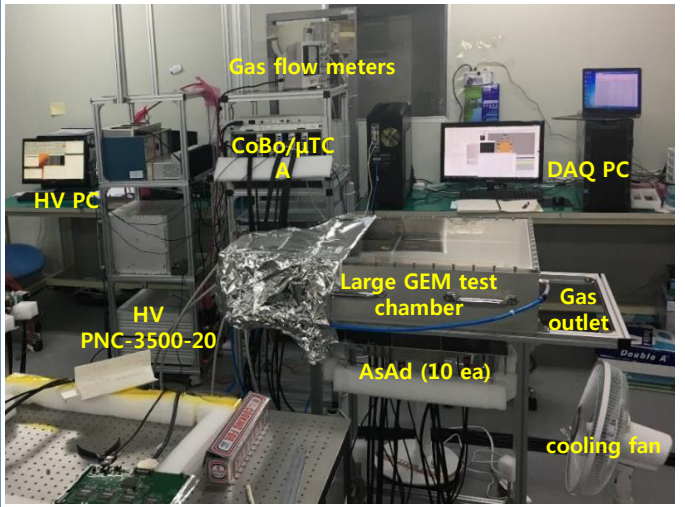


Threshold

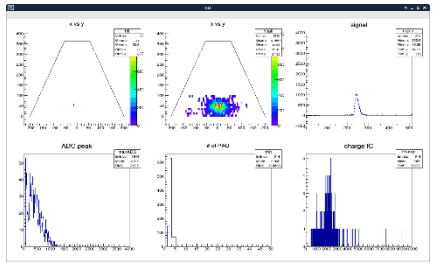


Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2 x 256 cells
Sampling Frequency	1 MHz to 100 MHz
Multiplicity	
Multiplicity signal	Analog "OR" of 64 discriminator outputs
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC [(3-bit + polarity bit) common DAC + 4-bit DAC/channel]
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit, selected or all
SCA Readout mode	1 to 512 cells
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64(68) channels; 1 internal test capacitor per channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel @ 3.3V

GEM test with GET system

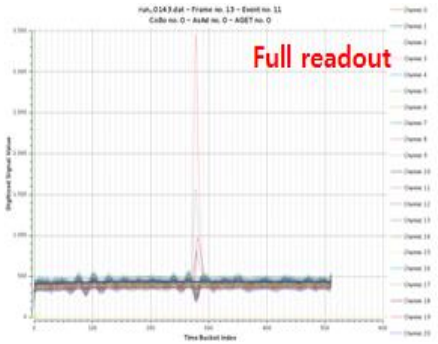


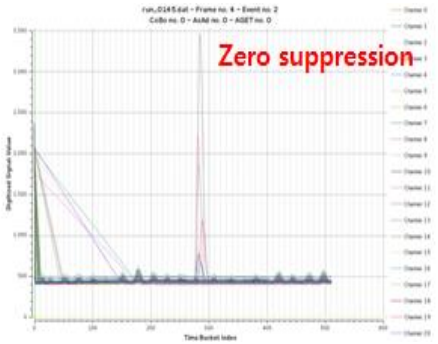
- GEM test with r-CoBo & M-CoBo system
- Self trigger : multiplicity mode
- Large GEM test
  - 3CoBo + 10AsAd
  - online monitoring

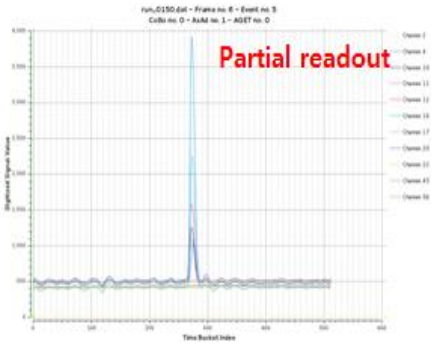


Prototype TPC beam test with GET system

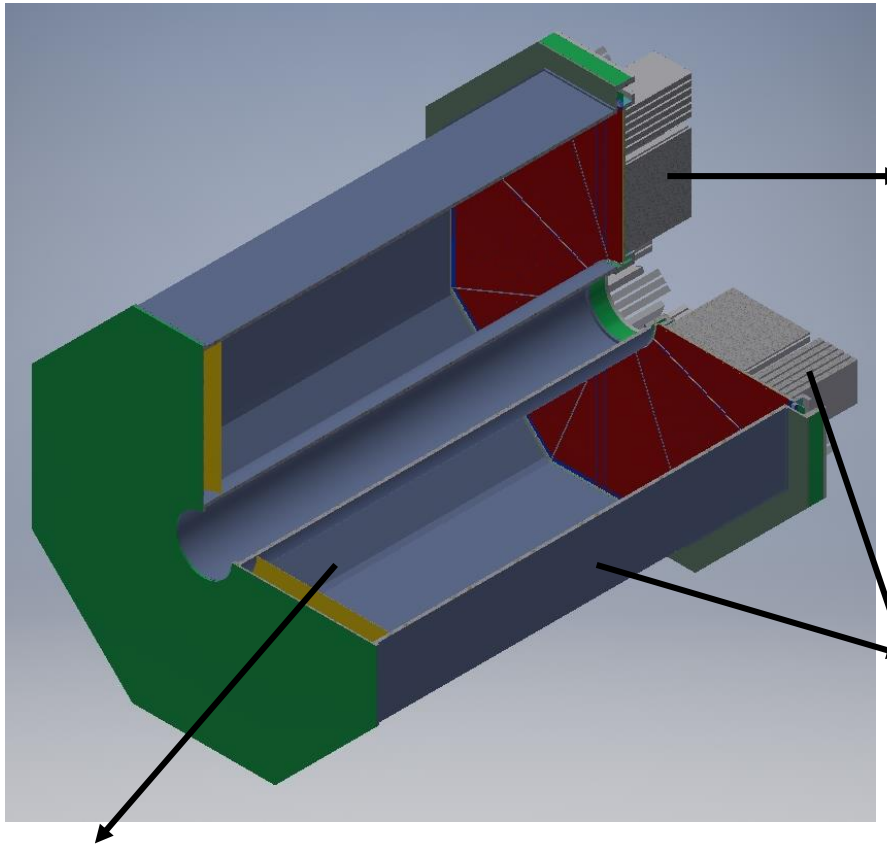
- Prototype TPC test with positron beam
- External trigger mode
- Test readout mode : full readout, zero suppression, partial readout







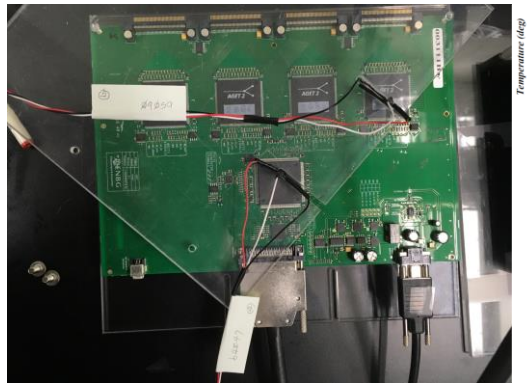
Control & monitoring system

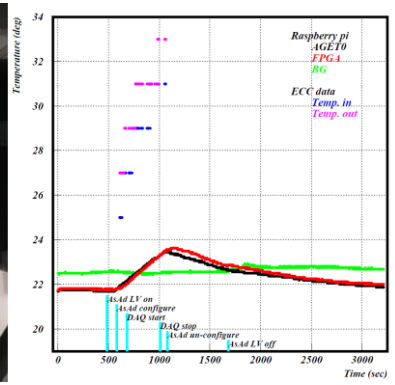


LV system for AsAd

- WIENER MPOD EC LV
  10slots, 3kW
- MPV8008I
  8V/10A, 8ch, 50W/ch
- MUSE control (network)
- Control program : c++ & perl/tk
- Ready for 120ch

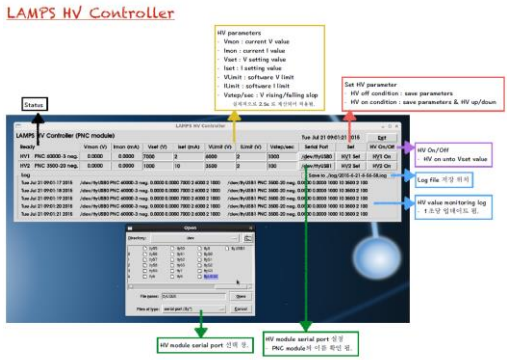
Temperature monitoring system for AsAd and TPC

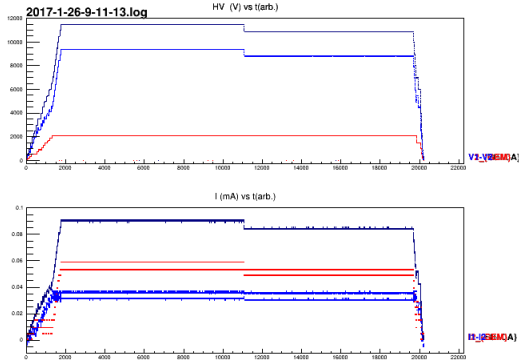




- Temperature sensor : DS1820
- Raspberry pi
- LAMPS TPC will use for front-end electronics and TPC chamber.

HV system





- PNC60000-3 : 60000VDC, 3mA
- PNC3500-20 : 3500VDC, 20mA
- RS232 interface
- 12bit for voltage and current monitoring
- Control program : c++ & perl/사
- Used for FC and GEM of prototype TPC
  for GEM test
- LAMPS TPC will use HV system for FC & cathode

Summary & Plan

- **GET system is ready**
  120ZAP, 120AsAd, 120cable, 30CoBo, 3Mutant

- **Readout PAD will be ready until 2019.08**

- **LAMPS DAQ system : ~2019**
  purchase : ~ 2019.08
  installation (part) : ~ 2019.10