Development of a high-speed detector readout system

D-RD-17

Francois Le Diberder, LAL Orsay, 10th May 2019

On behalf of the KEK-LAL team

Introduction

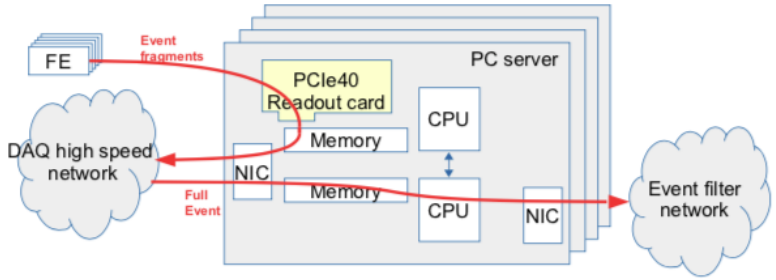
- Project between LAL and KEK to develop a system to readout a particle physics detector at high speed

  Initial proposal was submitted last year (funded).

- Implemented in the context of the **upgrade of the Belle II DAQ**
- Chose to use as hardware the **PCIe40** board developed for the **LHCb Upgrade by IN2P3/CPPM** (cf. L. Vacavant talk)
- Project consists in developing the necessary firmware

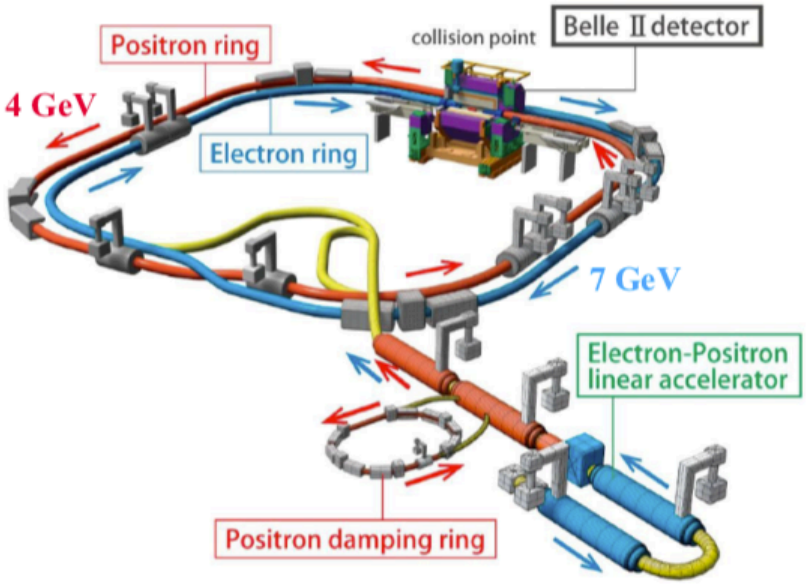
New directions in HEP DAQ

- Huge data rates are mandatory in particle physics experiments:
  - search for rare processes or precision measurements.
- Sophisticated trigger systems are required to digest these data:
  - Full detector information used
- Necessity to couple tightly data acquisition & computing resources for real time processing and high speed network
- Development of dedicated hardware, such as the PCIe40 board, which is collecting a large amount of data from optical input links, and hosted in PC servers to have access to CPU and network

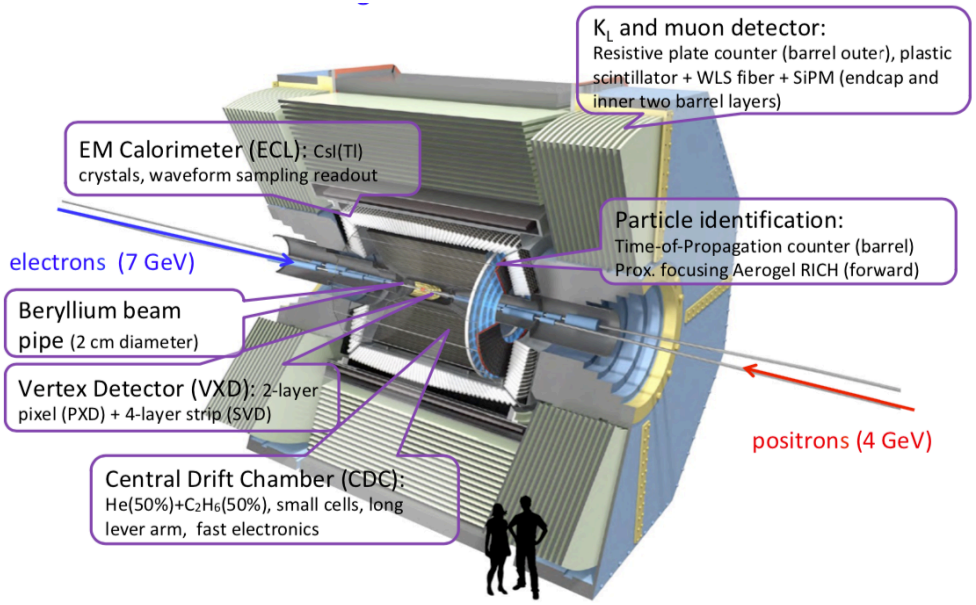


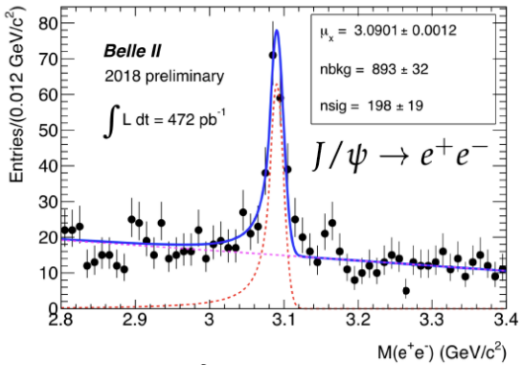
Belle II experiment

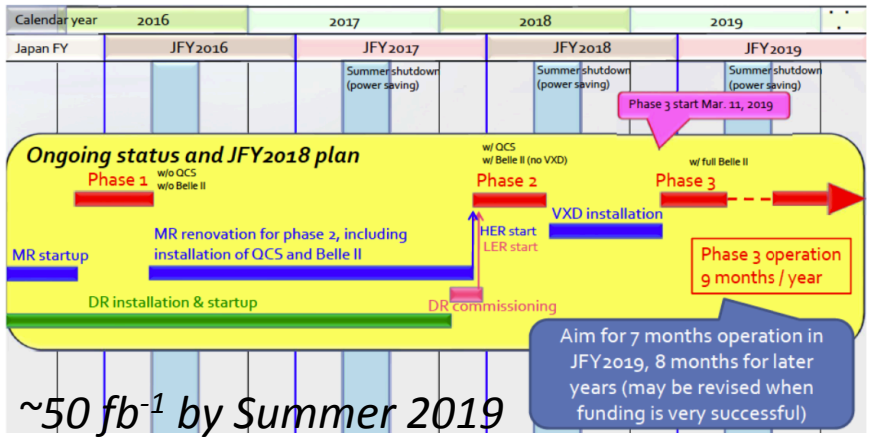
- Indirect search for New Physics in heavy flavour decays (B, D, τ) via precision measurements
- At SuperKEKB accelerator:
  - Designed luminosity: 40 times KEKB
  - Integrated luminosity of 50 ab^{-1} in 10 years (1 ab^{-1} for Belle)
- ~900 members from 26 countries



Belle II detector

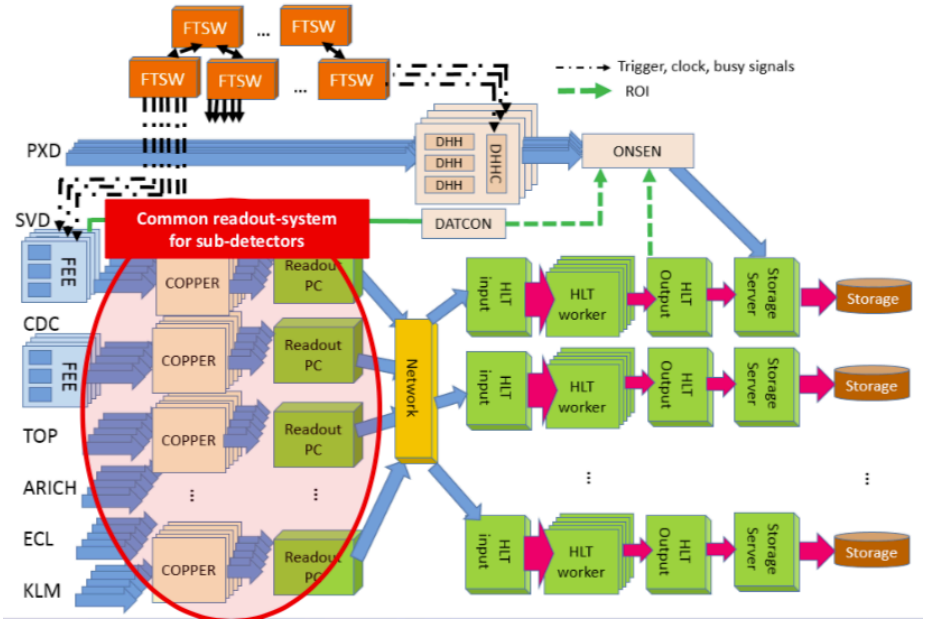






~50 fb^{-1} by Summer 2019

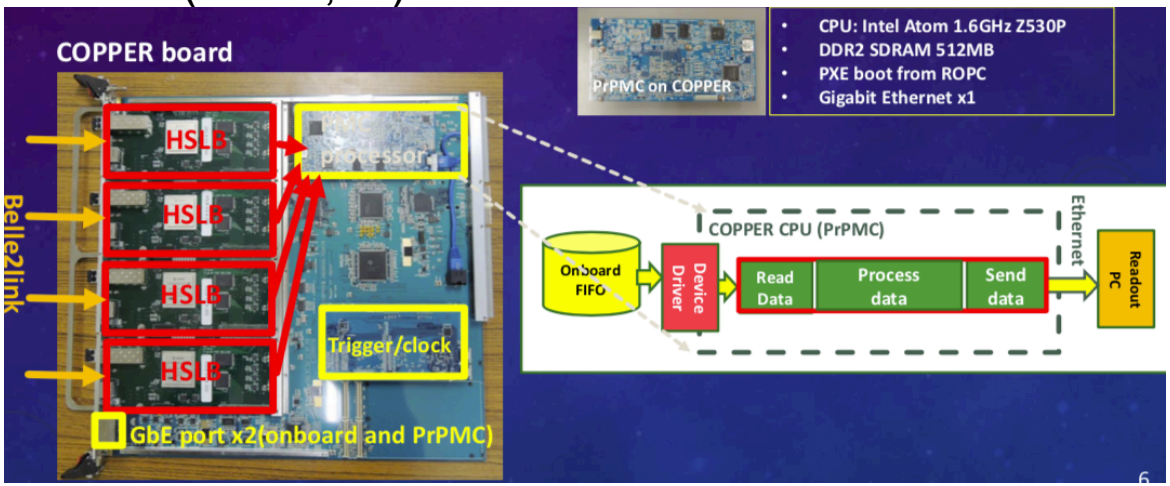
Belle II Current Readout System



- Common readout for 6 of the 7 sub-detectors
- Formatting, data-checking and partial event-building done in DAQ stage

COPPER boards

- COPPER is the common readout board for current Belle II operation:
  - Versatile board developed by KEK: same functionality as in Belle
  - Can be equipped with I/O and processor cards: new daughter boards are used for Belle II (HSLB, ...)

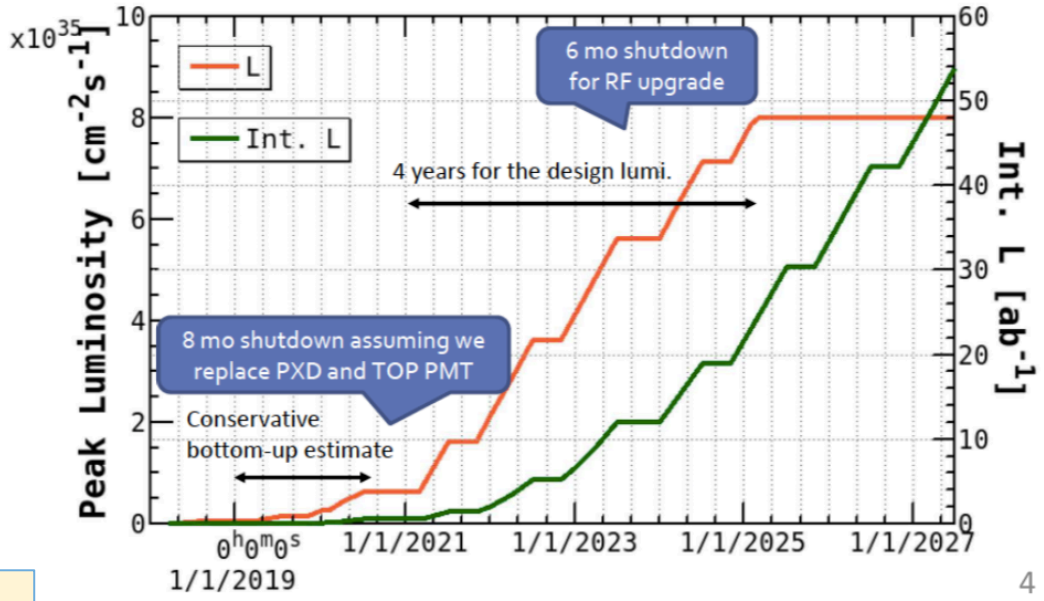


DAQ upgrade for Belle II

- Maintenance difficulty during the foreseen lifetime of the Belle II experiment
  - 4 different types of boards (COPPER, TTRX, PrPMC, HSLB) to take care of.
  - The number of spare components which are not available anymore is increasing.
- Limitation in the improvement of performance of DAQ
  - Bottlenecks of the current readout system:
    - *CPU usage*
      - About 60% of the COPPER CPU is used at “30kHz L1 trigger rate with 1kB event size/COPPER” (*i.e.* the Belle II DAQ target value).
    - *Data transfer*
      - 1Gbit Ethernet link per COPPER board.
  - We need to have a better readout system when:
    - *Luminosity* of SuperKEKB exceeds expectations.
    - *Lower thresholds* of L1 trigger required to improve the efficiency of low multiplicity events.

Upgrade schedule

- Belle II collaboration is now considering to replace the current readout system in time for when accelerator achieves target luminosity.
- The DAQ replacement will be performed using winter accelerator shutdowns.



2018-2019 Development and launch mass production

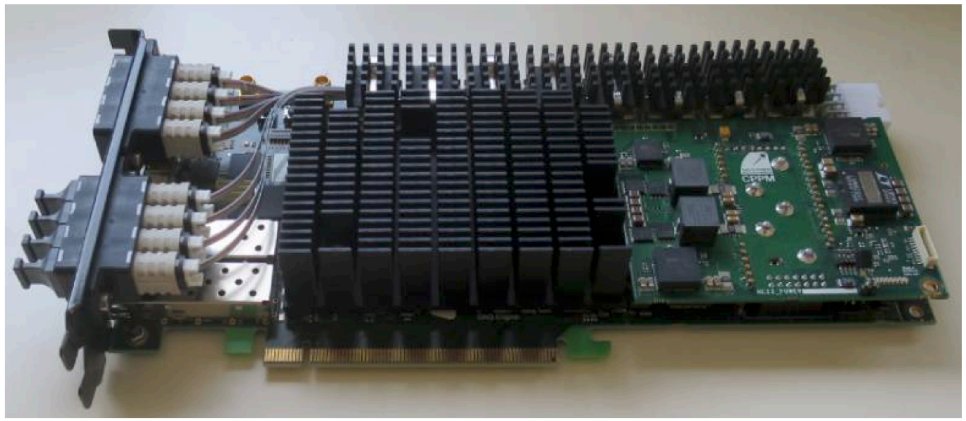
~2020 Installation

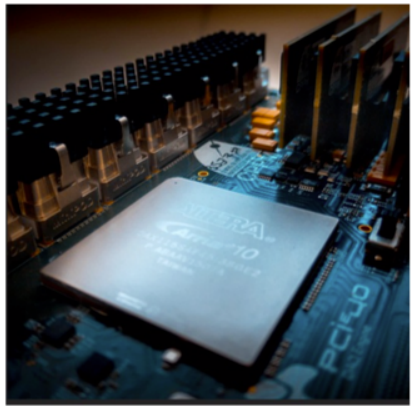
Requirements for Belle II DAQ upgrade

- Larger number of input channels per board:
  - From 4 to ~40 per board
  - Total system fits in ~20 boards
- Higher output throughput
  - Upgrade network to 10 GbEthernet
  - Data transfer via PCI express
- Larger buffers
  - Absorb fluctuations of throughput in computer memory
- Smaller number of board types:
  - All functionalities will be contained in a single board instead of several ones
- **Keep the current interfaces to other subsystem:**
  - **Format of optical links from Front-End to DAQ identical (Belle2link)**
  - **Data format to software trigger identical**
  - **Keep timing system identical**

PCIe40 board

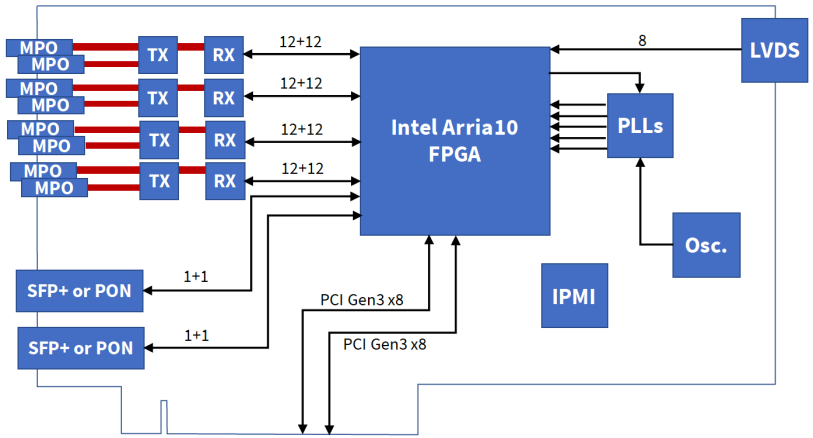
- Board developed for the LHCb Upgrade Phase I (Trigger-less readout at 40 MHz) by CPPM (Marseille) and CERN, used also by ALICE and Mu3E experiments
- Versatile hardware: possibility to use it for the Belle II DAQ upgrade is being evaluated by LAL-KEK collaboration: hardware fulfills all requirements, but firmware has to be developed



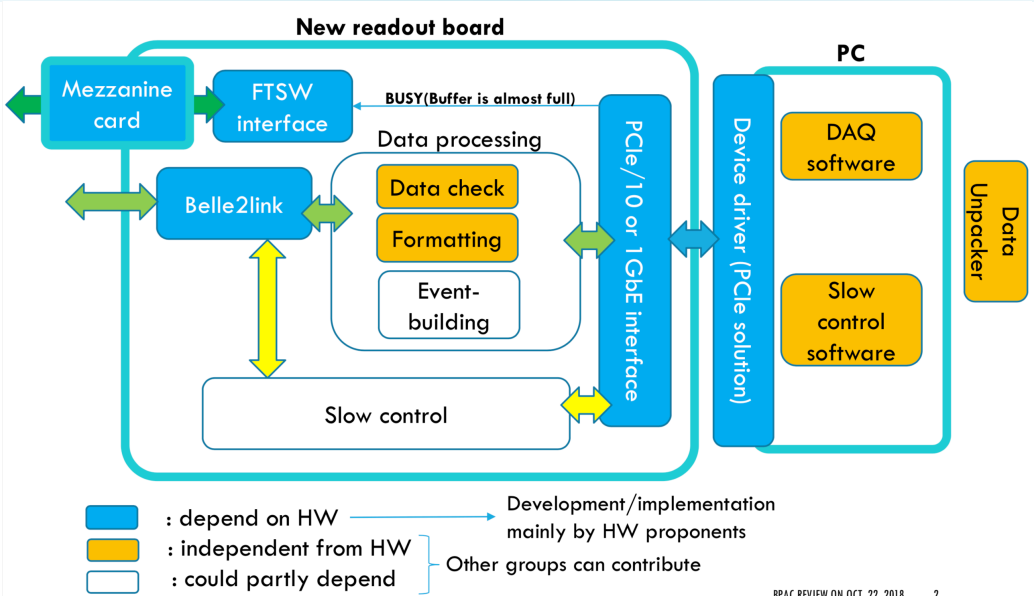


PCIe40 board

- Main features
  - PCI express board (hosted in server) with a large ***ALTERA ARRIA10*** FPGA
  - ***48x2 optical links*** running at 10 Gbits/s on mini-pods with MPO 12-fiber connectors
  - ***2 PCIe Gen3*** x8 interfaces to host server, tested at 112 Gbits/s



Firmware development



- Firmware needs to be developed to adapt PCIe40 to Belle II → Close collaboration mandatory.
- Common development between KEK and LAL groups, which both have large expertise in electronics development and operation of HEP detector DAQ.

Teams and activities

KEK	LAL
Satoru Yamada	**Daniel Charlet**
Ryosuke Itoh	Christophe Beigbeder
Mikihiko Nakao	Eric Jules
Qidong Zhou	Emi Kou
	François Le Diberder
	Eric Plaige
	Patrick Robbe
	Monique Taurigna

Request:
KEK : 1500k¥
Granted:
IN2P3 : 30k€

- Regular video meetings between the development teams to share work
- Visit of Nakao-san to LAL in December 2018 to implement timing interface in PCIe40 board
- Several important milestones achieved together by the two teams: readout of Belle II Front-End electronics (CDC, ARICH) by the PCIe40 board and interface to the timing system.
- Next meeting in KEK, mid June 2019 (set-up of a demonstrator on site).

Conclusions

- Collaboration between KEK and LAL established in 2018 to evaluate solutions for the upgrade of the Belle II readout system.
- A solution based on the PCIe40 board (CPPM/LHCb) fulfills all requirements.
- Development of firmware is needed, realized also in collaboration between the two groups.
- The exchange of expertise allowed to obtain already important results in adapting the PCIe40 board for the Belle II case.
- **Will be ready for October 2019 : selection decision**