NEWS ON THE CHIP-ON-BOARD PCB

FRONT ELECTRONICS FOR CALICE SIW ECAL

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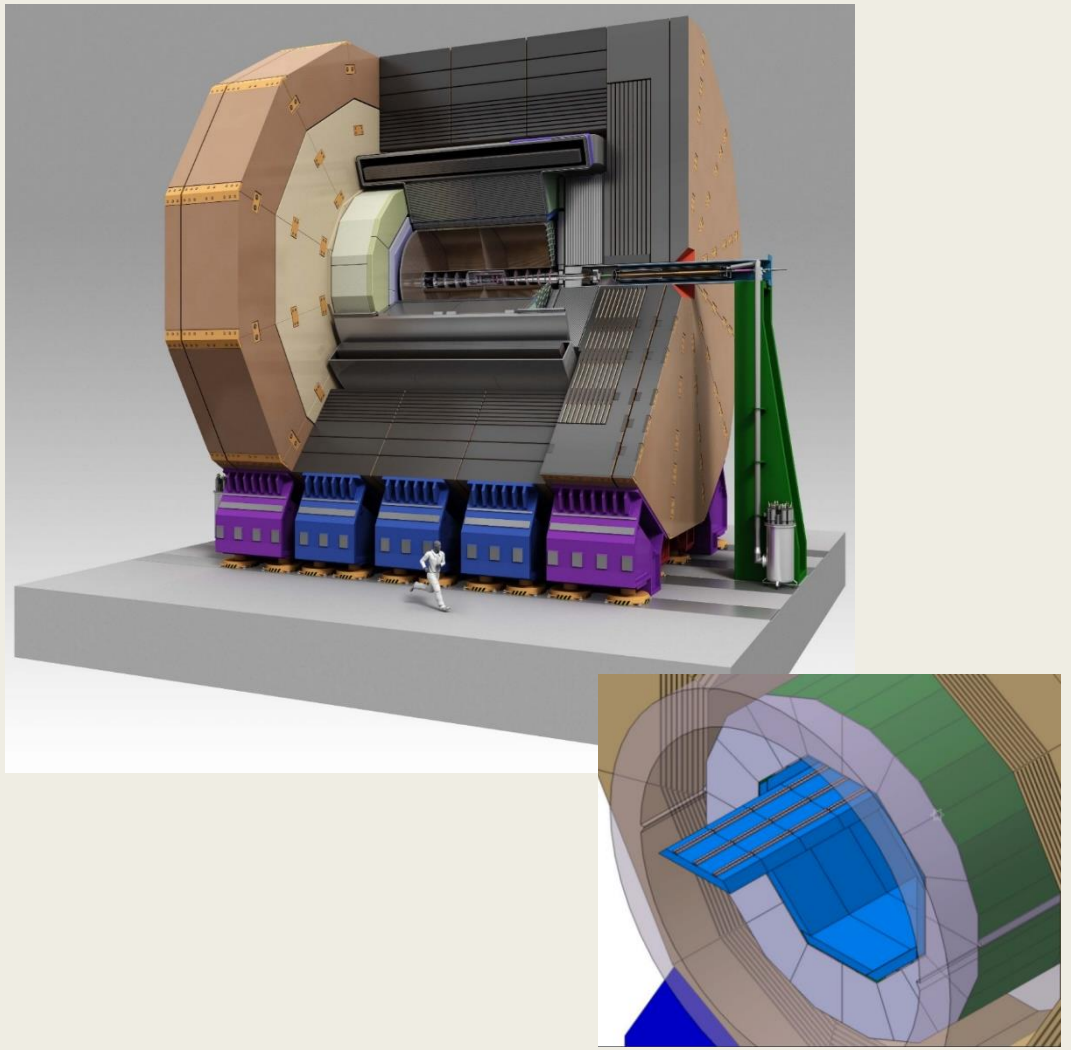
My talk

- Introduction
- Motivation
- Process on the FEV-11 board fabrication
- Injection test
- Ultra- flat Capacitors (LAL Group)
- Summery

Introduction

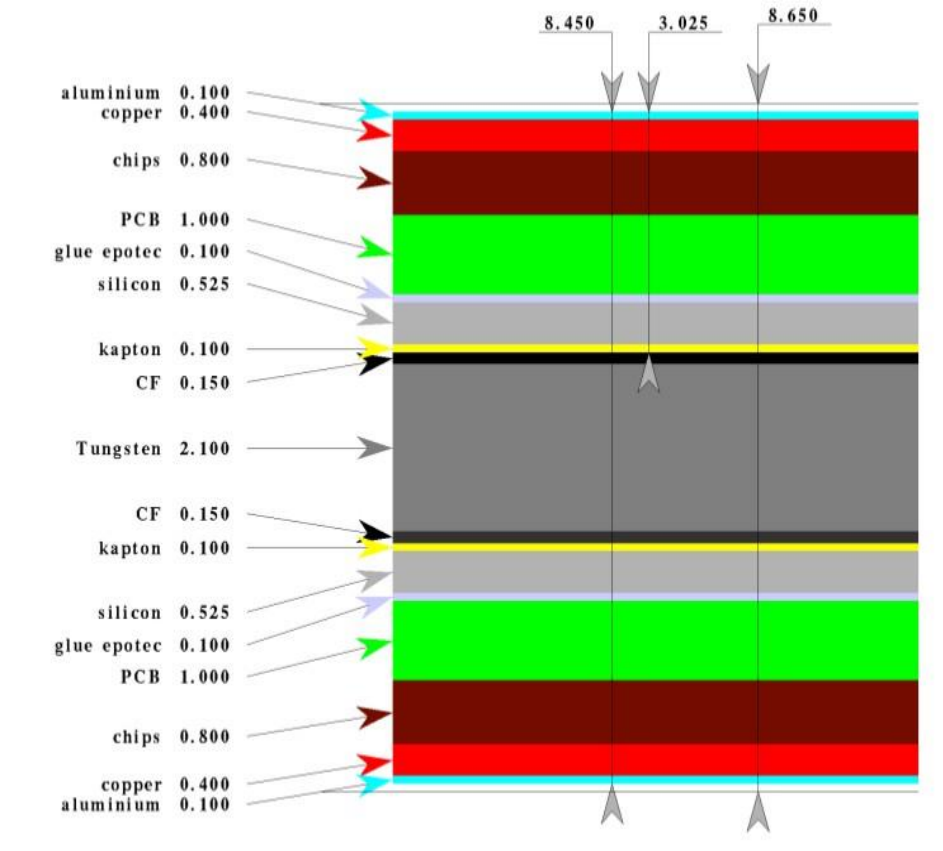
- Latest status of developments proposed by LAL, Omega and SKKU group for a Silicon-Tungsten electromagnetic Calorimeter (SiW-Ecal).
  - Ultra thin PCB: Chip On Board

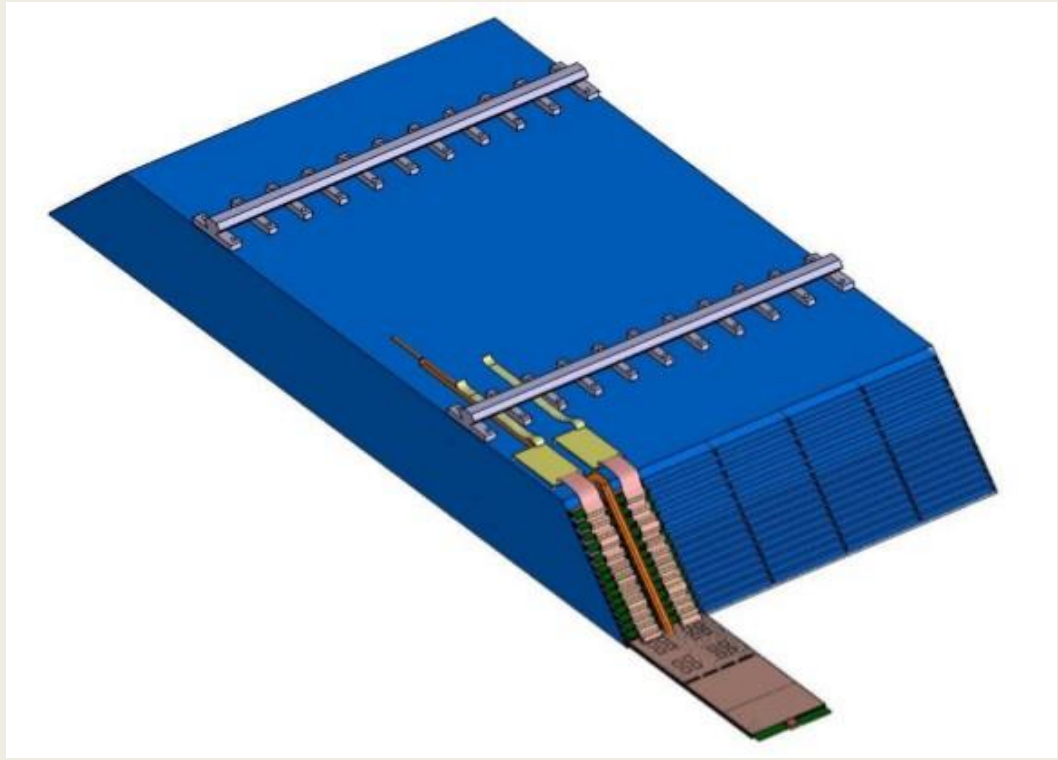
- Electronics developments is done by:
  D. Breton, J.Maalmi, J.Jeglot.
  - Power Pulsing: Proposal to use new ultra-flat super-capacitors on all ASUs of the Slab (order 10 ASUs per slab).
  - Control and Readout Electronics: Proposal for a compact Slab digital interface board and Control & Readout module



Detectors for high precision physics at the TeV scale

Motivation



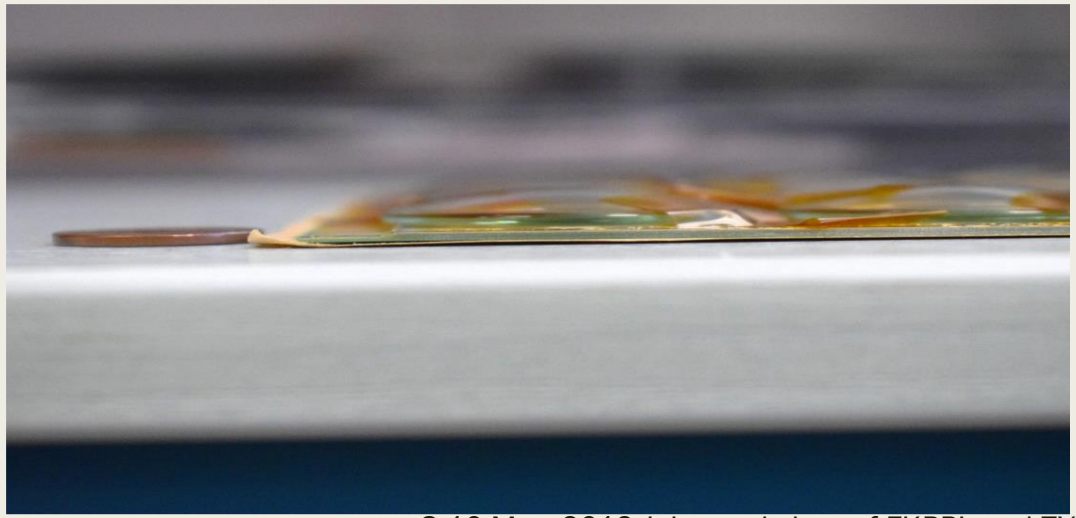


Drawings by Henri Videau for SiW Ecal Technical Design Document

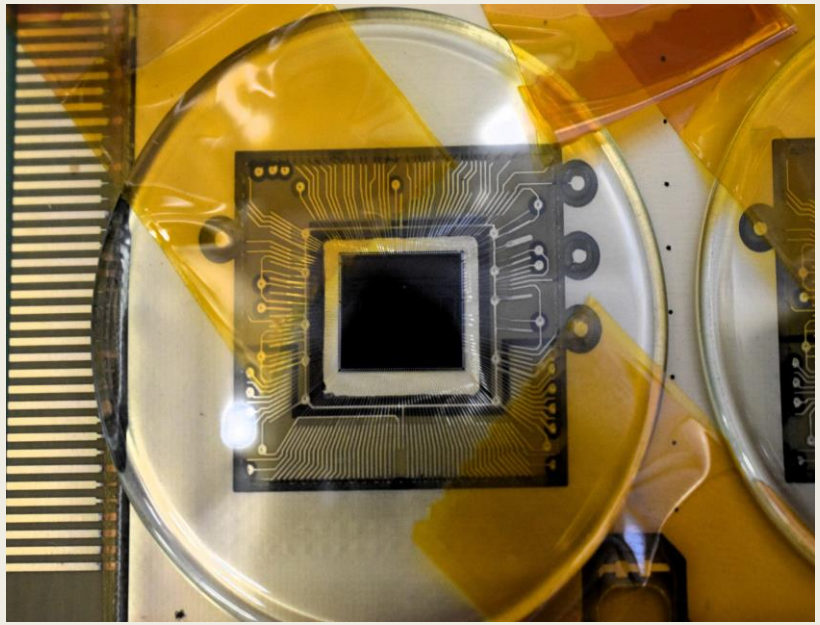
- Design: Total space for ASICs and PCB 1.8mm (was 1.2mm since ~2007)

Ultra thin PCB: Chip On Board

- **LAL & OMEGA** collaboration with **ITAEC/SKKU** (Sungkyunkwan University, Suwon – Korea) and **EOS company** for the PCB production.
- 10 FEV11_COB produced.
  - 1.2mm thickness → 9 layers PCB !
  - Good Planarity (metrology made in LAL) and electrical response.
- **4 boards wirebonded** at **CERN** bonding lab. Also In contact with CAPTINNOV Platform.

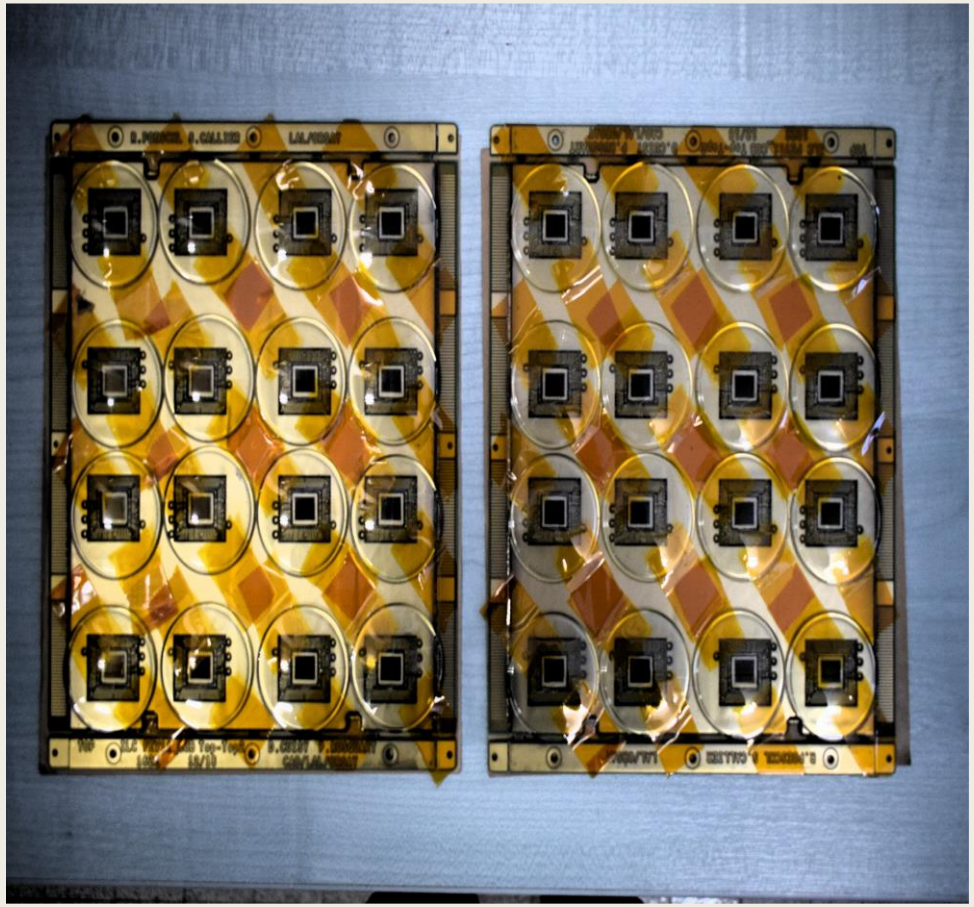


SK2a

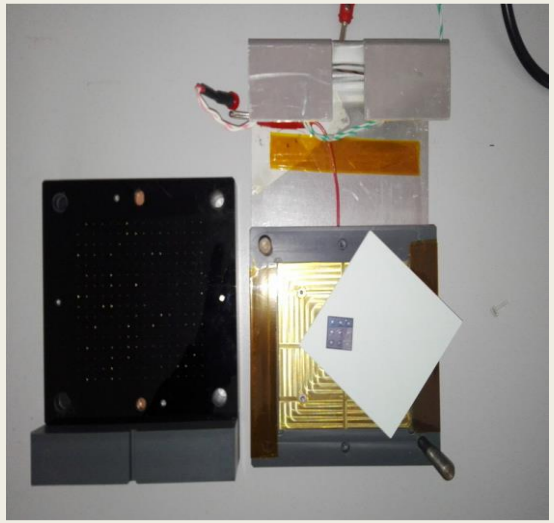


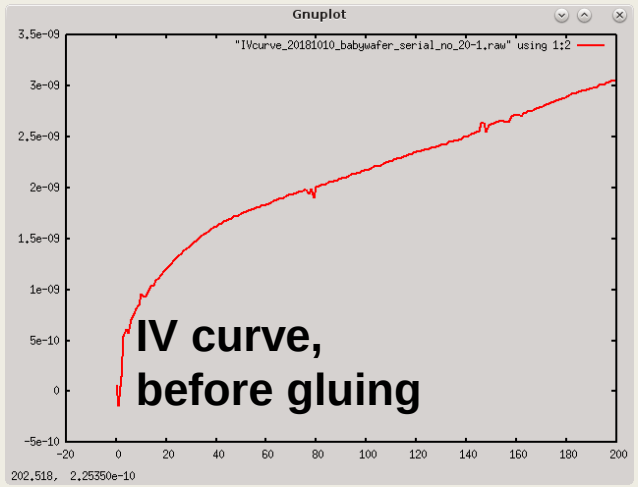
Ultra thin PCB: Chip On Board

- **Tests** ongoing since April 2018:
  - FEV11_COB: all chips respond and are configured (with SMBV4+DIF system and also SL-Board).
  - FEV11_COB: equipped with 3 baby wafers. Most of the following results are obtained with this board.
  - FEV11_COB. Just been wirebonded last month.

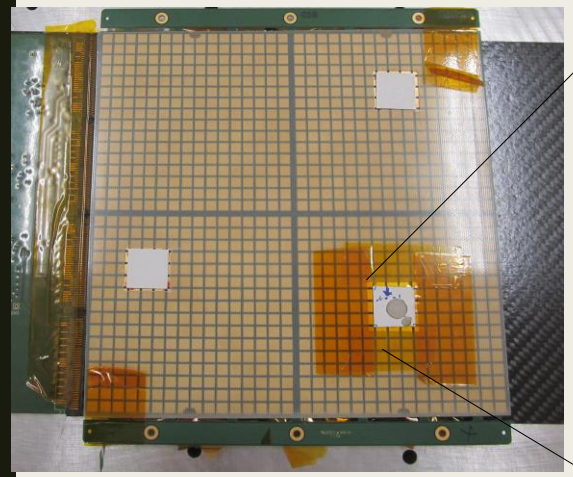


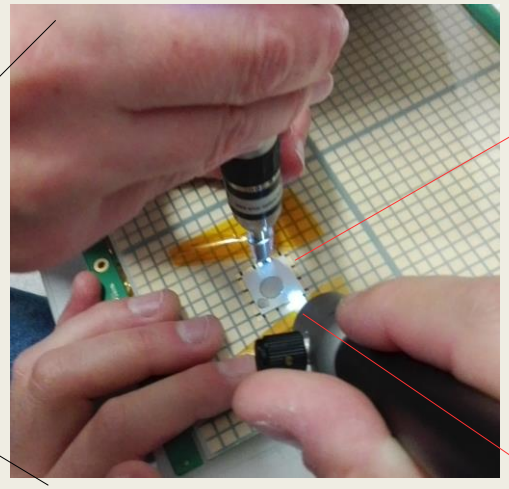
Baby wafer gluing

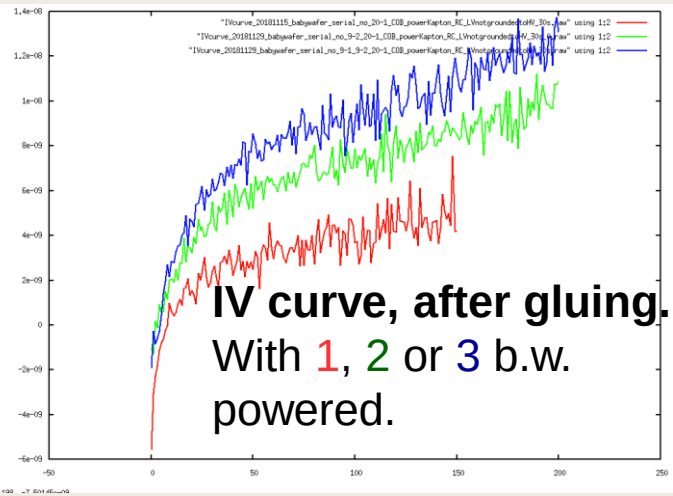




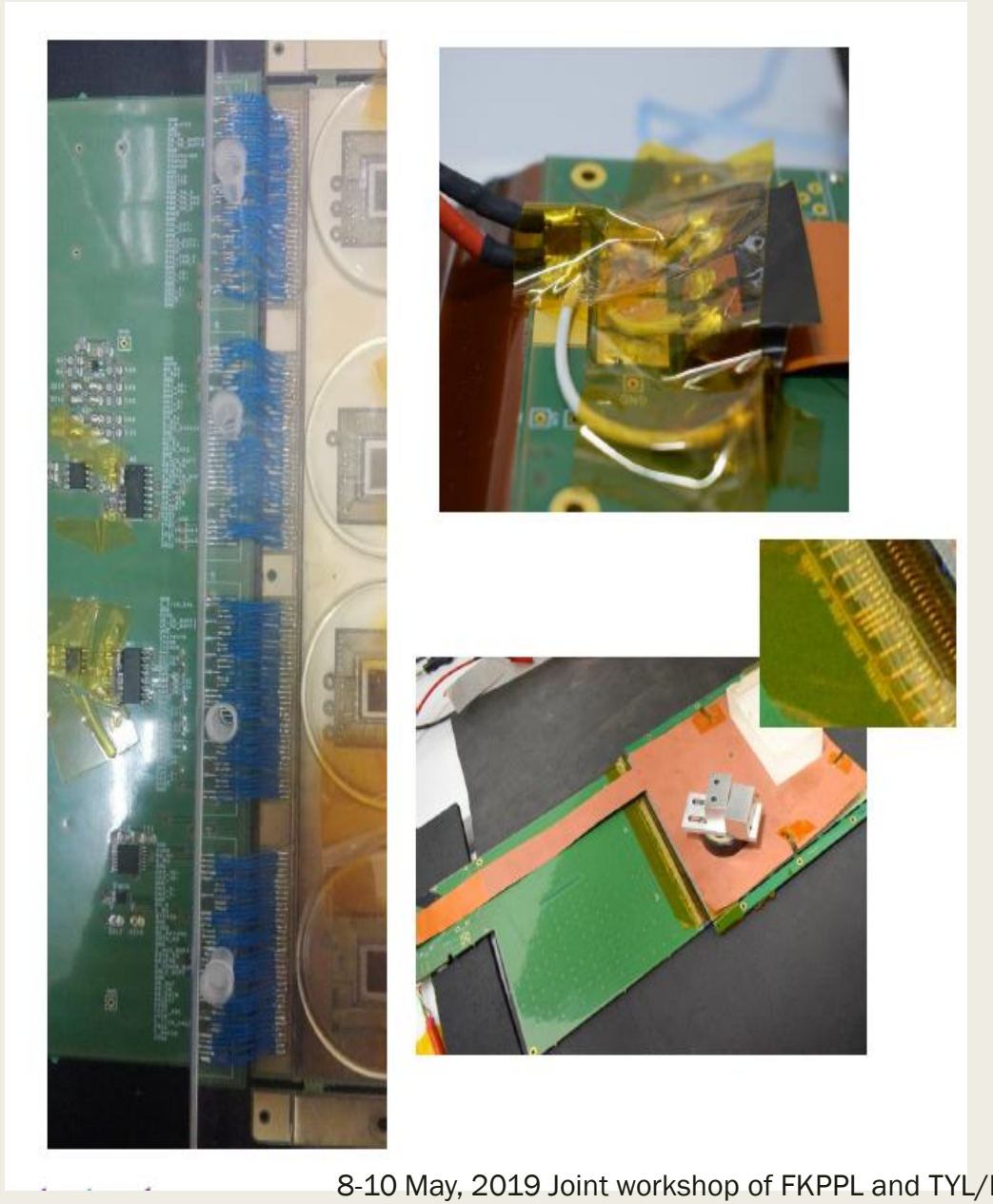
- We got a bunch of S10938-1364(X) “old” baby wafers (split guard rings, 4 rings, cut size B) of 3x3 pixels from T. Suehara.
- IV test bench borrowed from LPNHE. New expertises acquired at LAL (exported to Captinnov). Full wafer characterization will be done at LPNHE.
- The entity of sensors, thin PCB (printed circuit boards) and ASICs (application-specific integrated circuits) is called Active Signal Units or **ASU**
- 3 baby wafers manually glued.
  - *Visual inspection of the glue dots (light fiber system).*
  - *IV curves after gluing.*







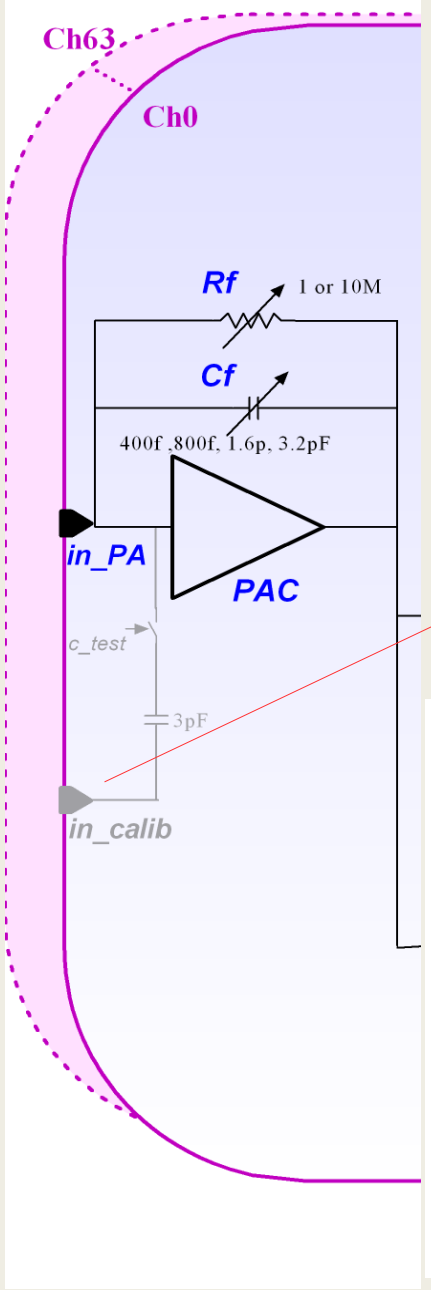
Test bench

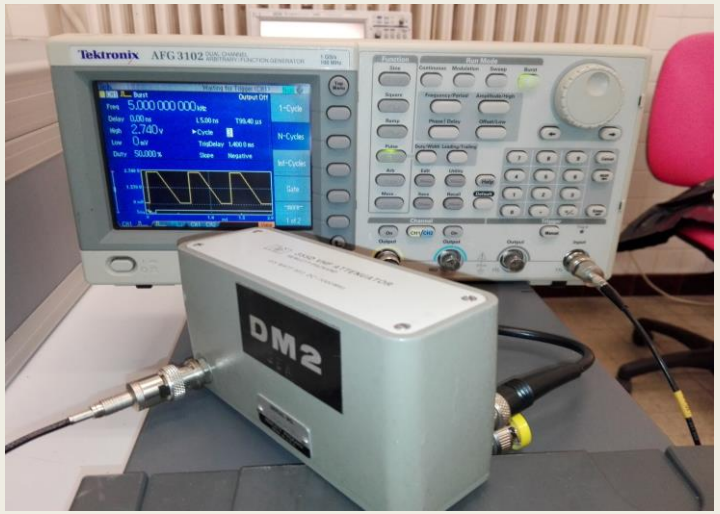


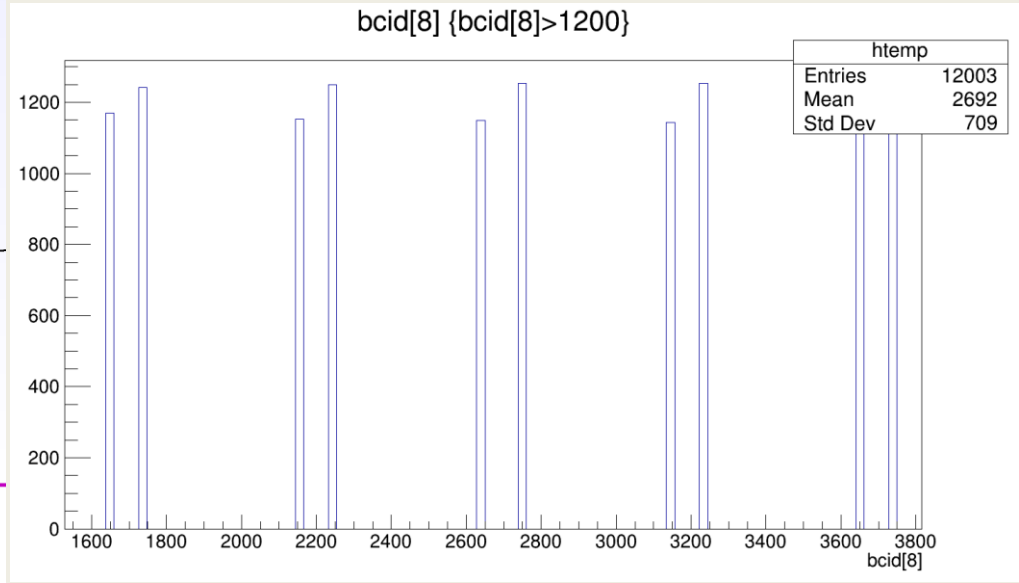
- FEV11_COB wire bonded to SMBv4 (+ DIF)
  - Modification of an SMBv4 prepared for the tests of individual ASU BGA based using temporary connections by pressure.
  - These connectors were optimized for thicker ASUs… Solution: wire bond the ASU and SMBV4.
- HV directly connected to the kapton sheet connectors (small RC fitler added).
- The baby wafers are polarized by direct contact with the kapton sheet.

Injection tests

- Tests injection signals equivalent to 1-0(100) MIPs
  - *Assuming Si sensors of 320 ± 15μm.*
  - *And that a MIP traversing the PIN parallel to its normal will create ~ 80 h + e −pairs per μm → ~4.1fC in total.*
- Pedestal measurement:
  - *We inject in one single channel per ASIC and we disable the triggers of all the others.*



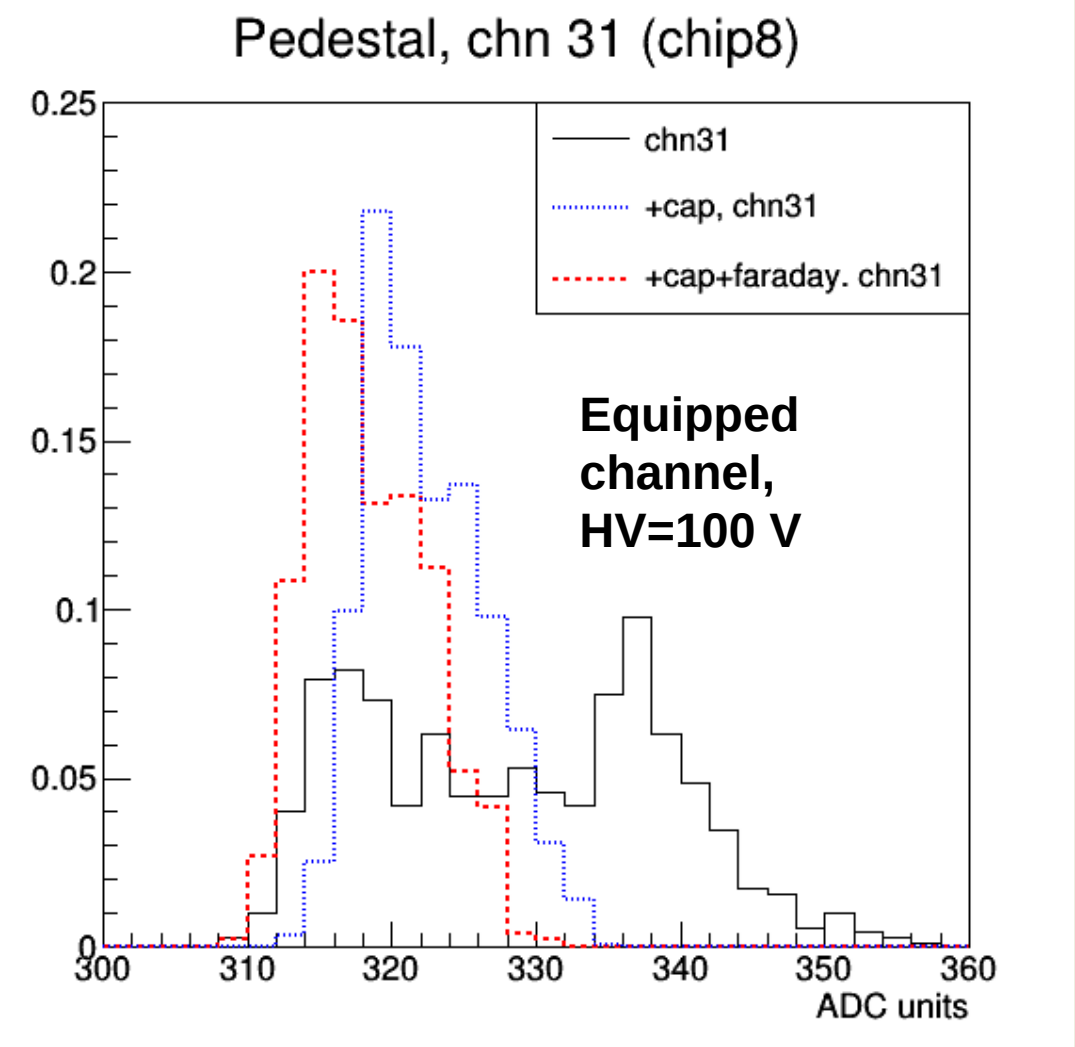




Brunch crossing identifiers (BCID)

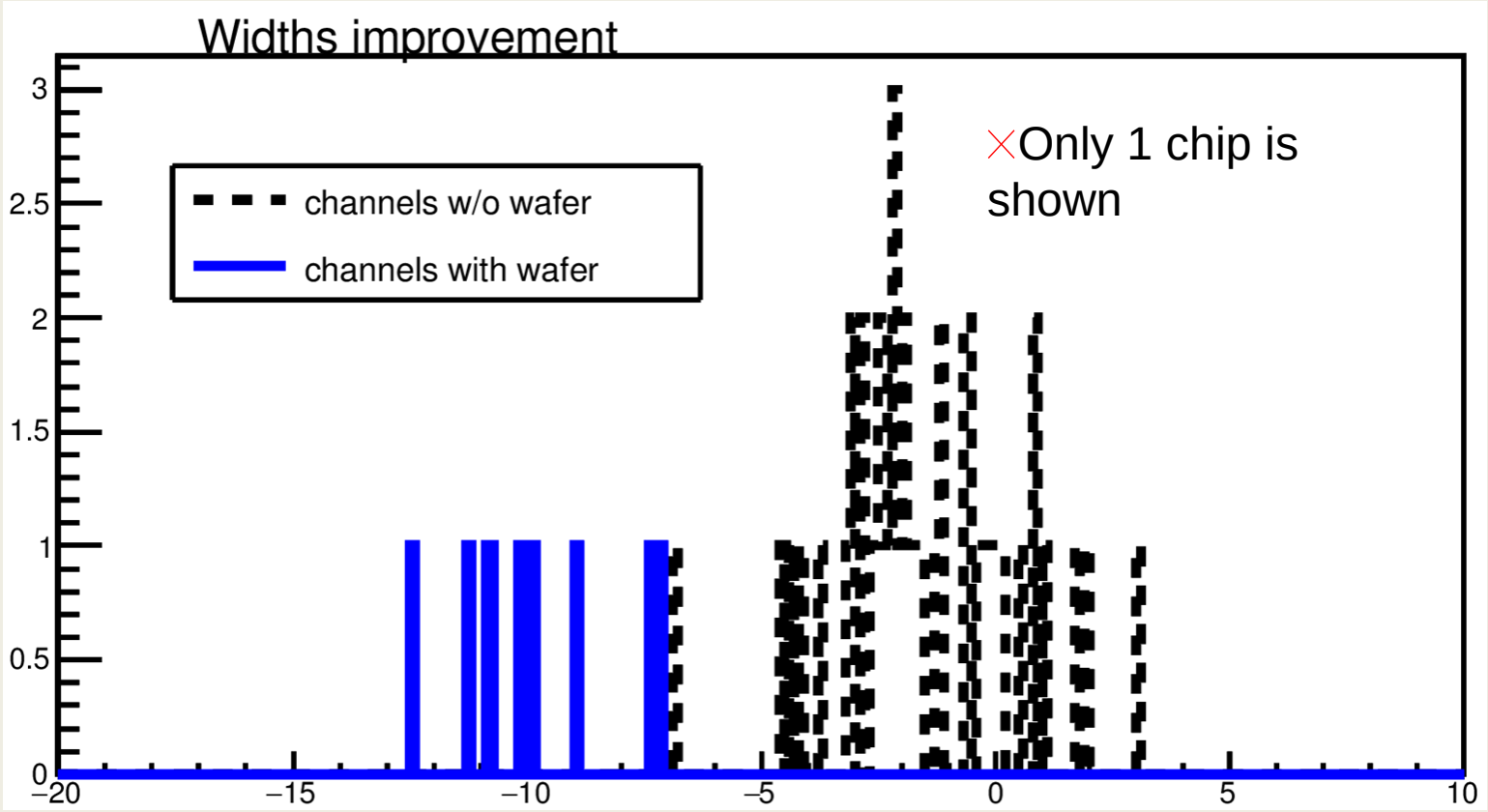
Injection tests (pedestal study)

- First pedestal studies showed wider pedestal distributions compared with the expectations.
- This effect is much larger for channels connected to sensors.
- To minimize this effect, we improved the HV delivery and light isolation +:
  - *Add AVDD and DVDD decoupling capacitances at the end of the SLAB (blue curve)*
  - *Further improvement on the HV delivery, light and electrical shielding (red curve)*



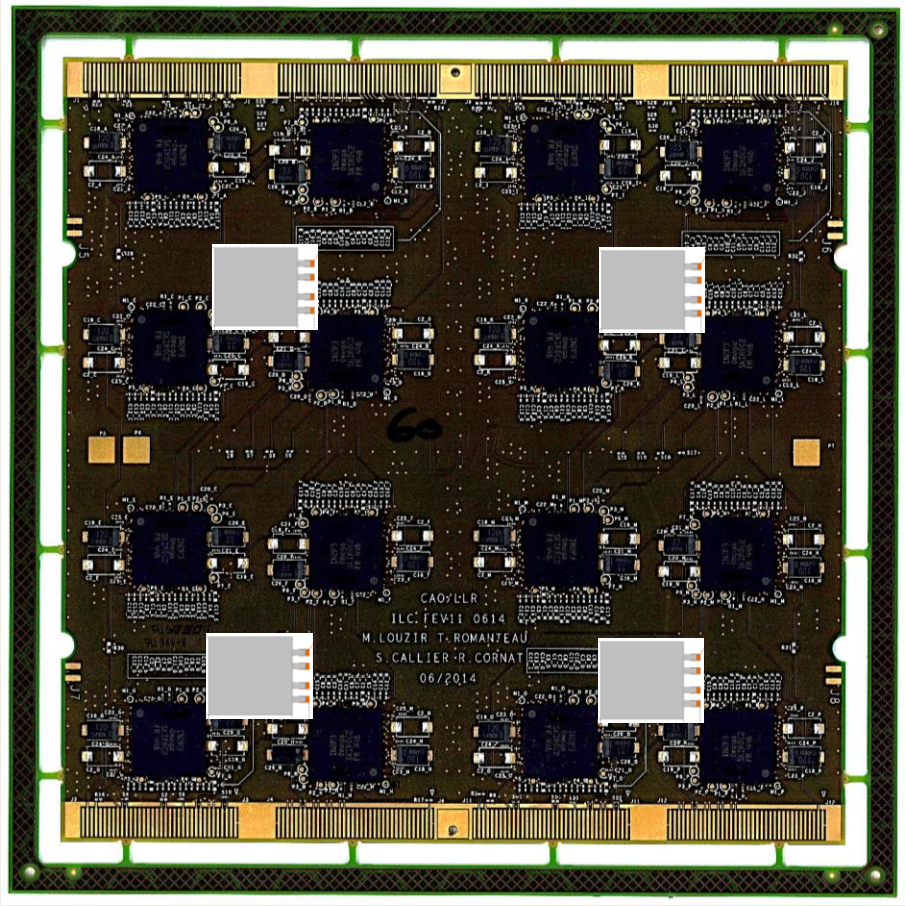
Injection tests (pedestal study)

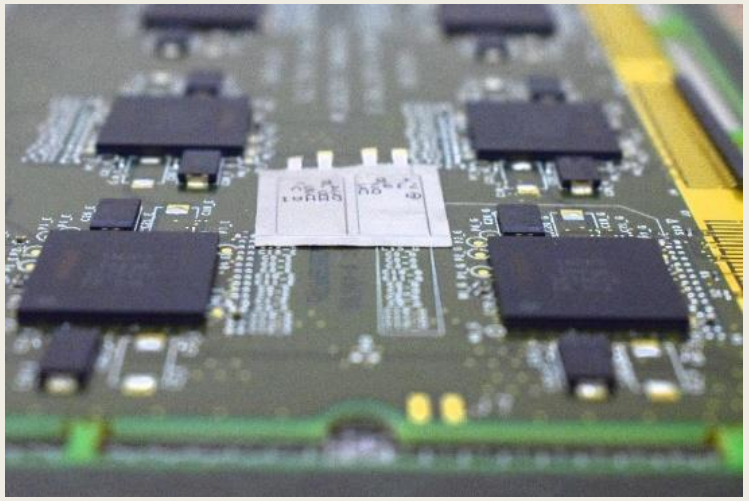
- What is the improvement in the width of the pedestal for each channel?
  - *Width defined as the RMS.*



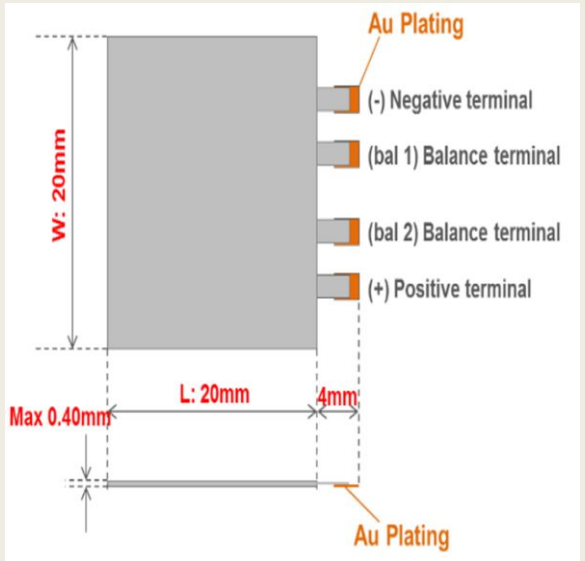
Ultra- flat Capacitors

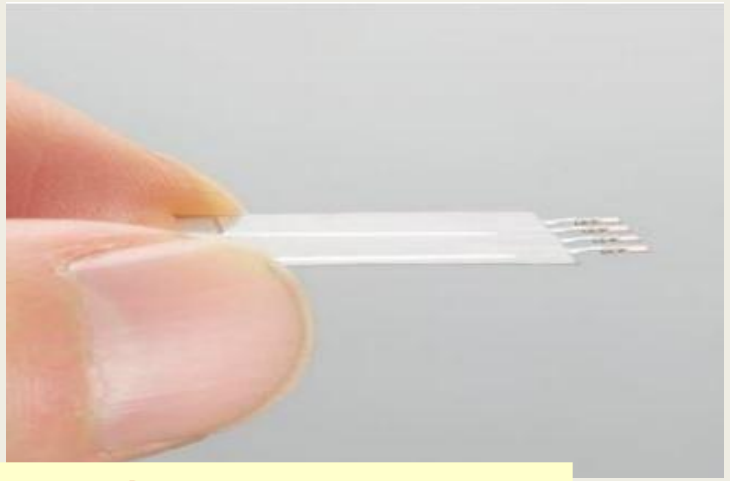
Ultra-Thin Supercapacitor
DMH series DMHA14R5V353M4ATA0
35 mF / 4.5 V





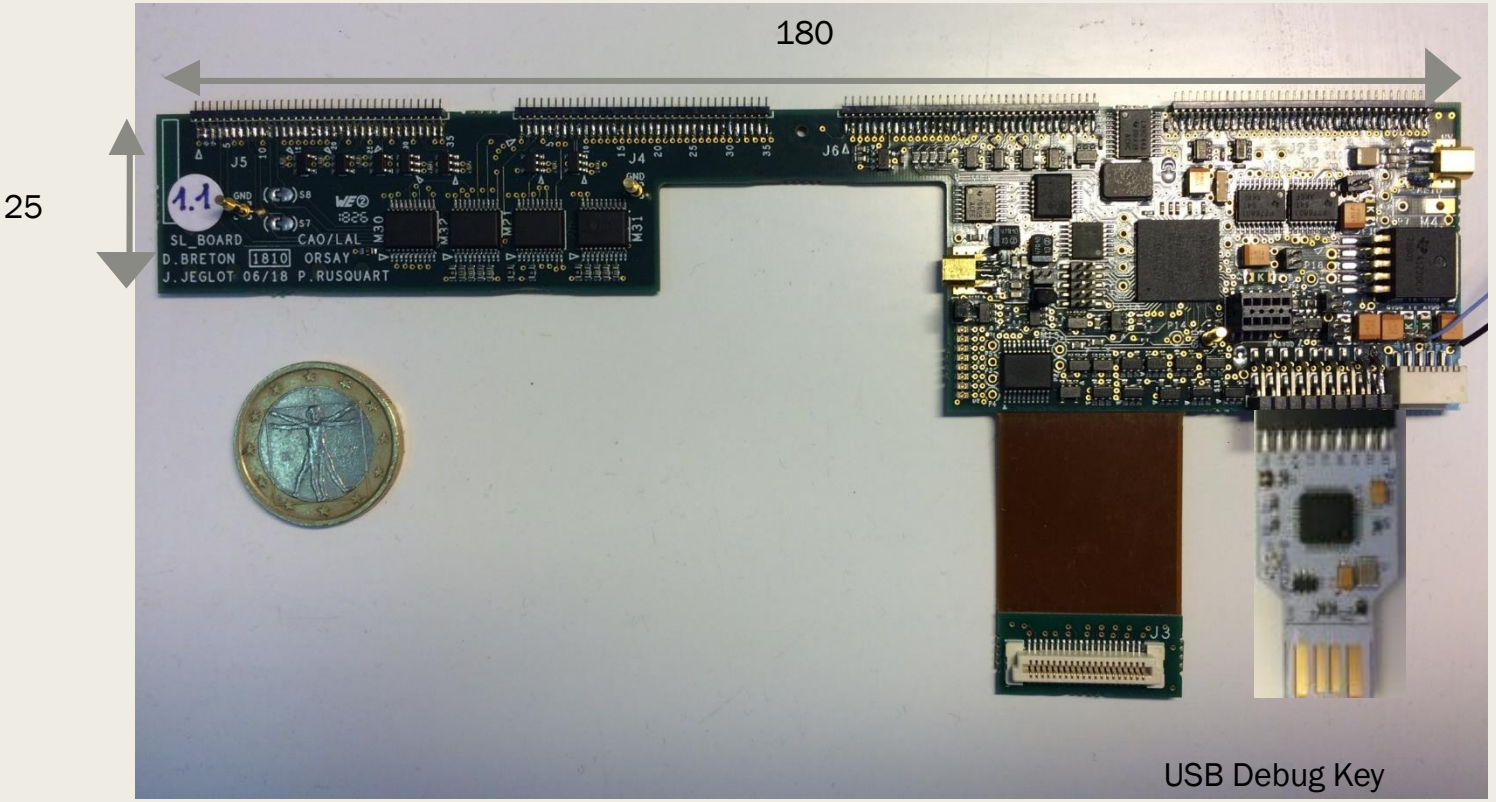
Integrated capacitors permit the peak current of ~1.5A to be local
during power pulsing => recharge is limited to a total of ~150mA …





Life time has to be checked, depends on voltage and temperature…

Status of development: SL_board



TEST OK

- USB communication
- Jtag programming
- Test ADC Vref Extern
- Test interconnection
- **Slowcontrol**
- **(16 skiroc2a on COB and BGA version)**

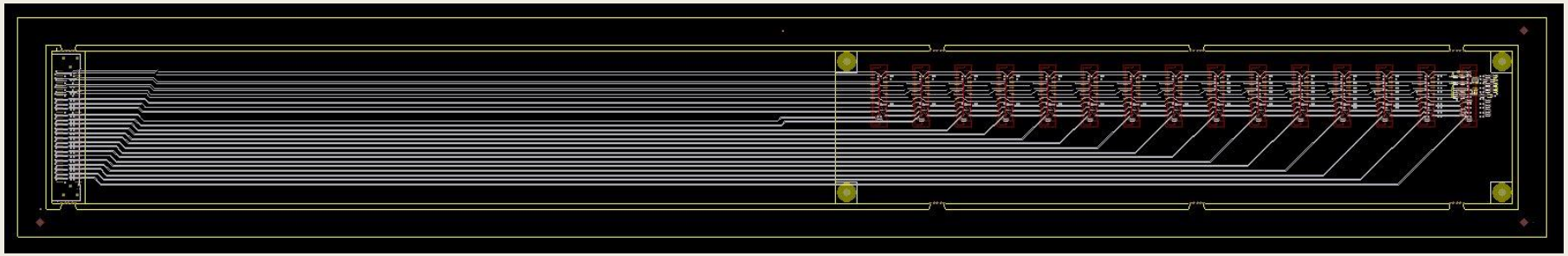
Status of development: CORE_kapton

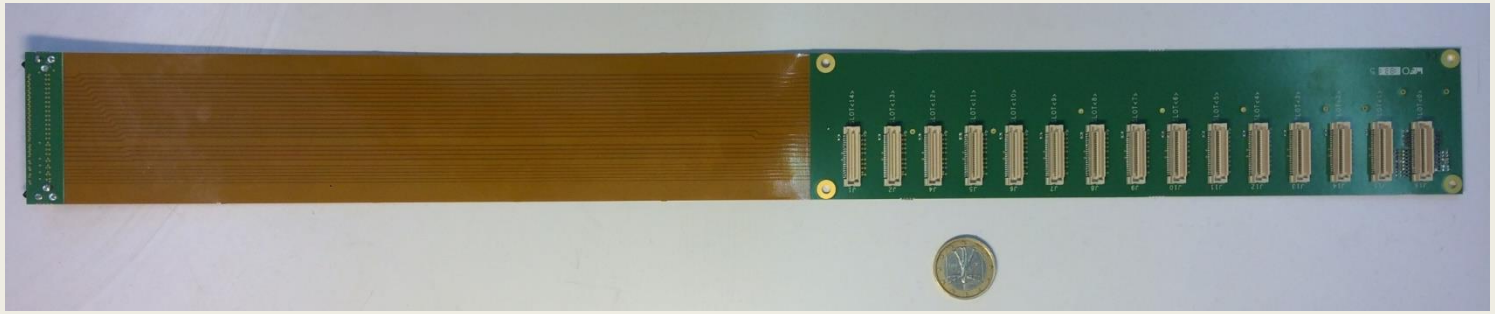
Total length ~45cm

CORE side

Flexible kapton

Slab side (~22cm, rigid, pitch of 15mm)



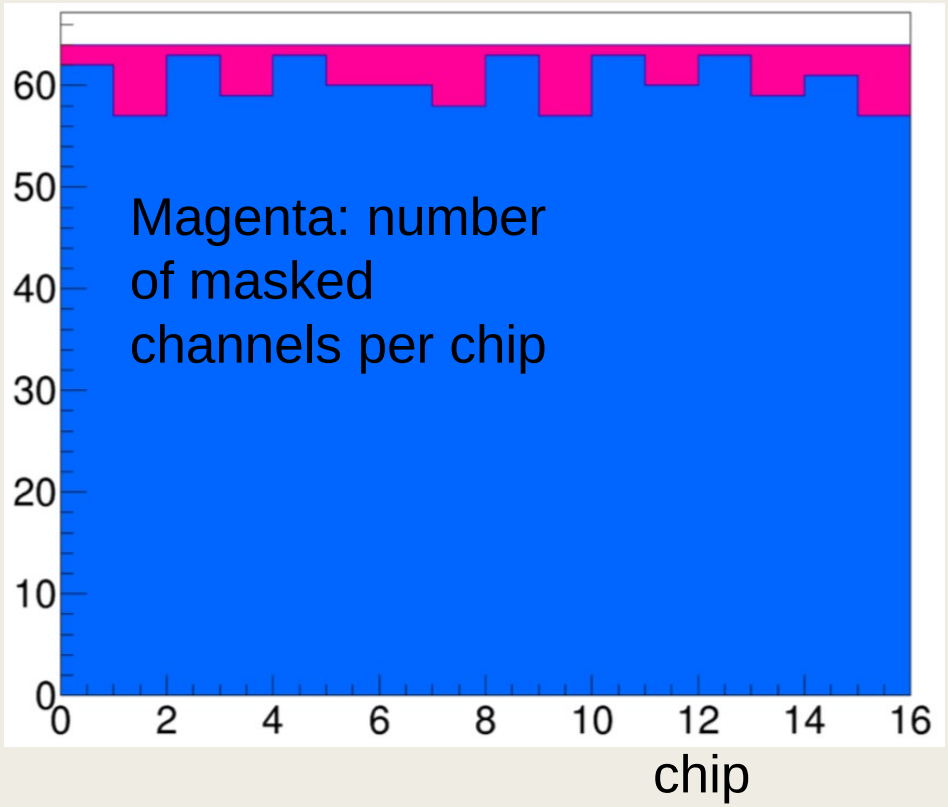


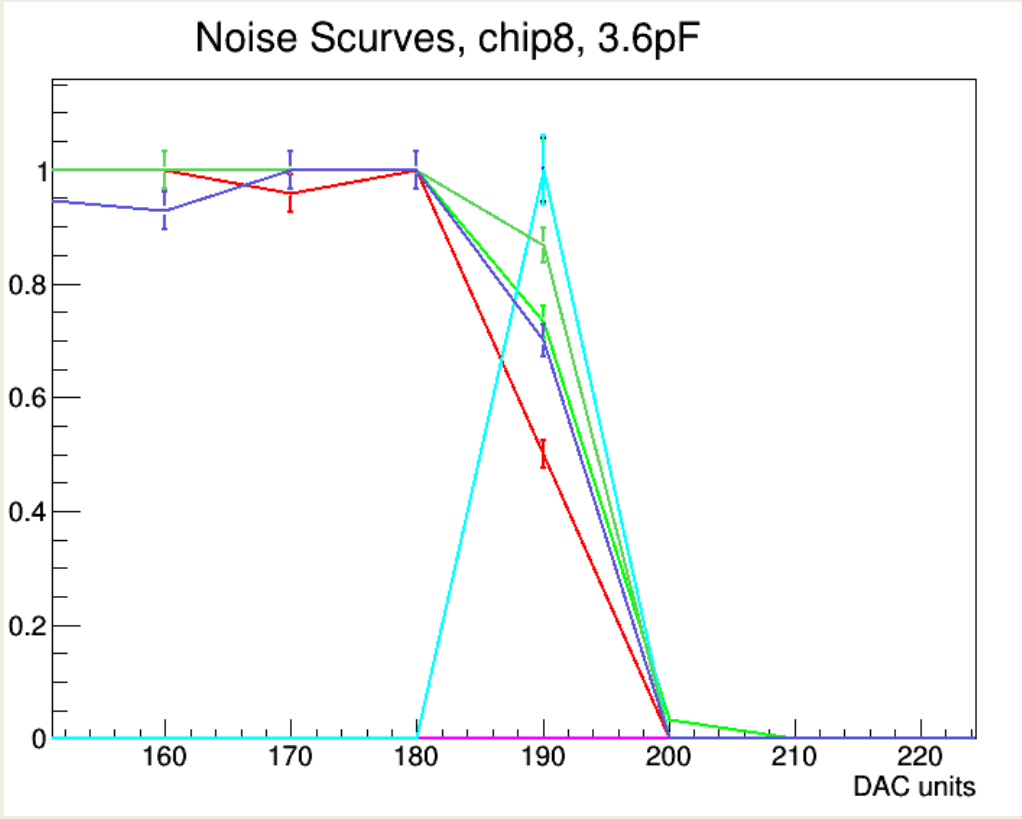
Core Module connector (100 pins):
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

SL_board connectors (40 pins):
7 common differential pairs for sensitive signals, *1 individual pair* for control and readout, 14 common lines, GND

Threshold optimization + noisy channels masking

- ~4% of noisy channels masked
- Threshold scans made with all other channels enabled.

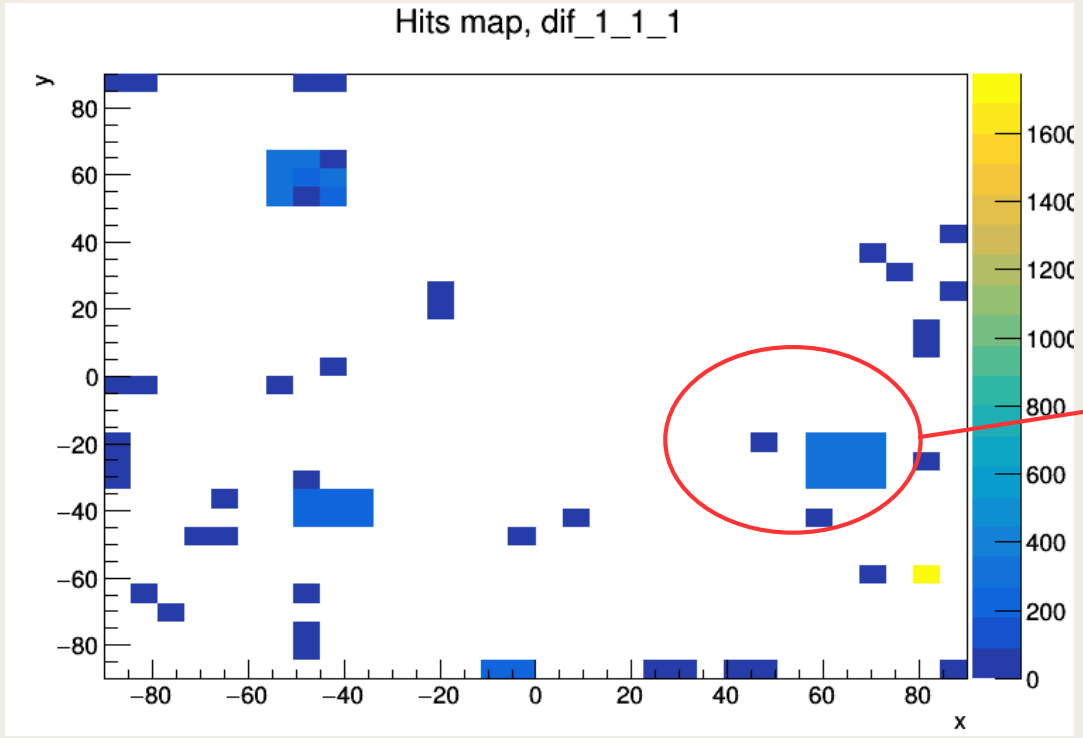


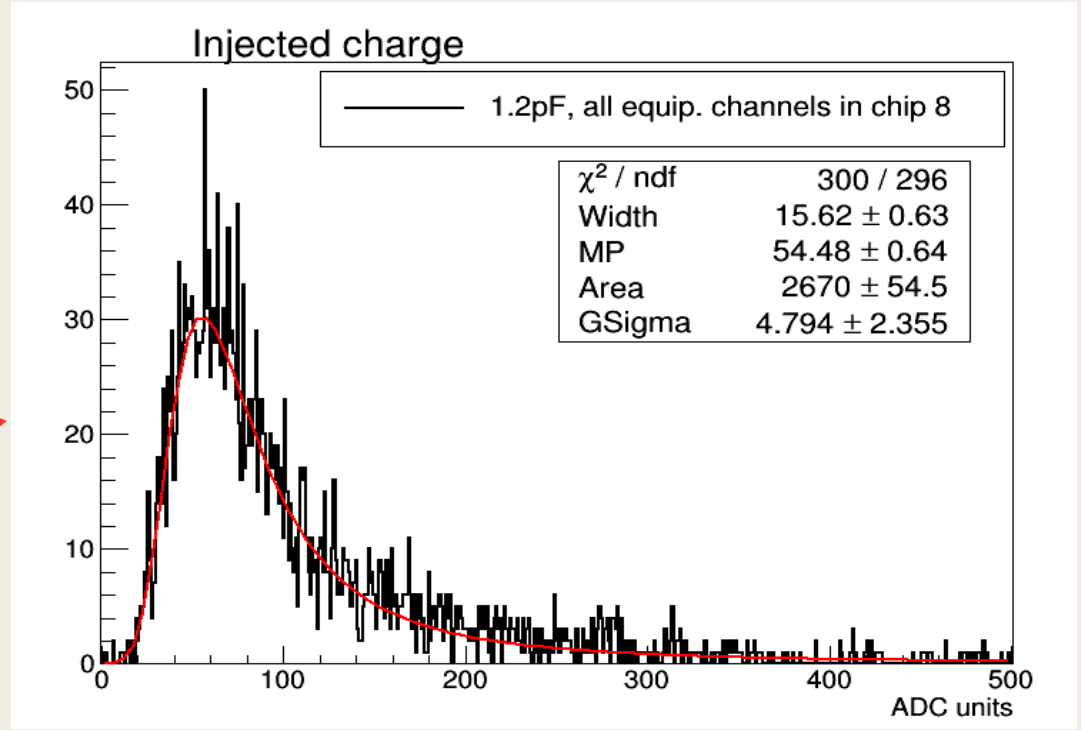


Only equipped channels are shown

Cosmic data

- Using settings from the commissioning described before

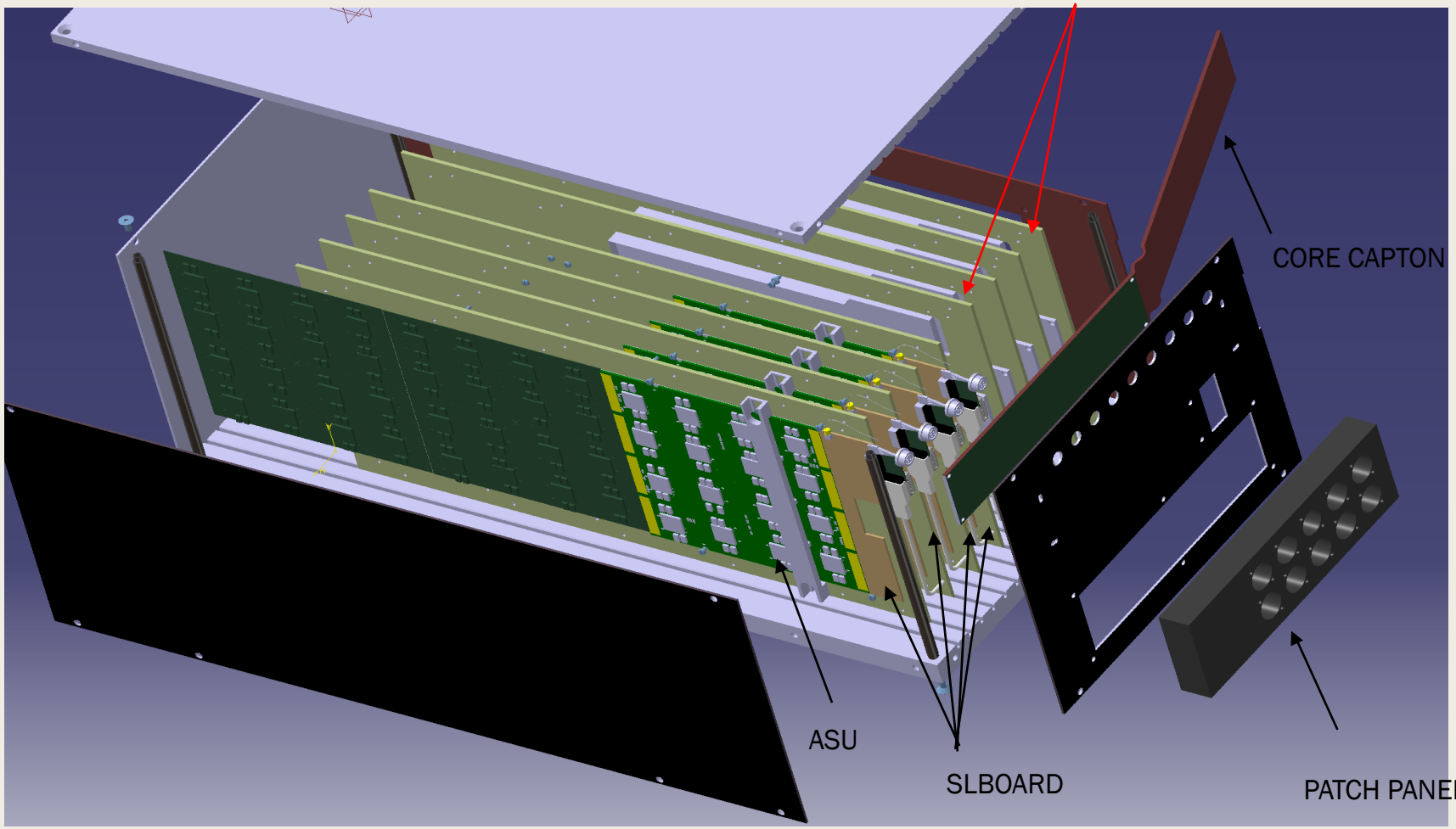




Status of development: TESTBEAM SETUP

4 SLBOARD WITH ASU COB AND ASU BGA

FREE SPACE TO INCLUDING *Kyushu* SETUP (fev13 Jp +smbV5)



Summery

- The COBs are fully functional and nicely recording cosmic ray data.
- Ready for wafer gluing
  - *LPNHE got a naked COB to test the feasibility of the gluing using the robot. Positive results of the test.*
  - *COBs are been tested with SMBV4+DIF and also with the new SL-board DAQ system.*
- Next beam test plans: produce and commission two COBs with glued wafers and connected to SL-boards. See Roman's talk.

THANK YOU FOR YOUR ATTENTION