D_RD_16

Development of Advanced Monolithic Pixel Detector

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Outline

Introduction
Collaboration Status
Recent Progress
- Japan
- France

Summary

Collaboration Members

France

Marc Winter*
Auguste Besson
Jérôme Baudot
Maciej Kachel
Christine Hu-Guo
Andreï Dorokhov
Frédéric Morel
(IPHC/IN2P3)

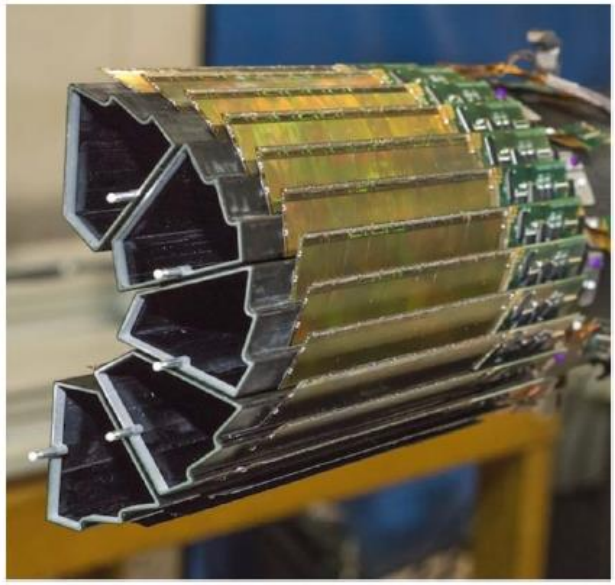
Japan

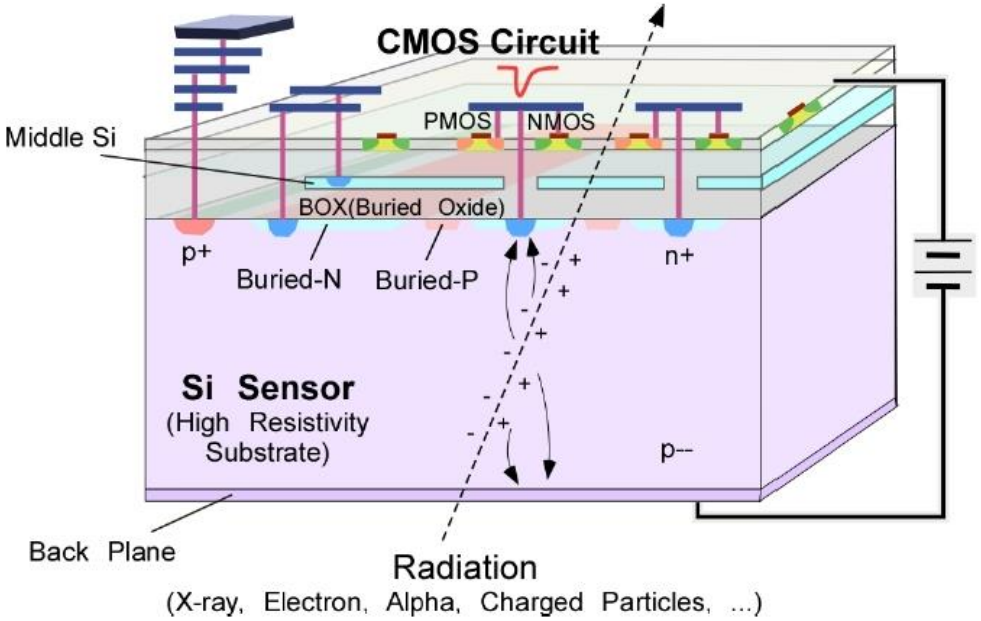
Yasuo Arai*
Ikuo Kurachi
Shunji Kishimoto
Manabu Togawa
Toshinobu Miyoshi
Toru Tsuboyama
(KEK)
Kazuhiko Hara (Tsukuba Univ.)

* PL

Collaboration (2017~)

CMOS sensor development





Long experience
in CMOS pixel sensors
Acc. exp: STAR-PXL(BNL),
ALICE-ITS(LHC), etc.

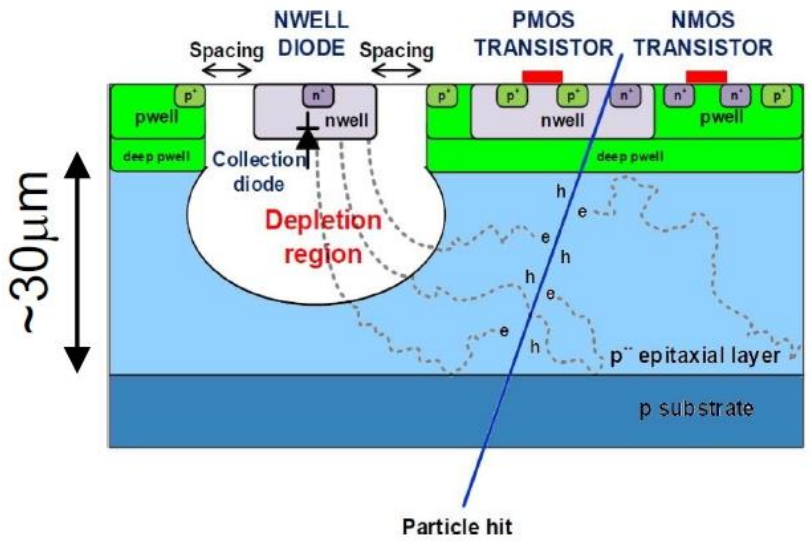
Bulk CMOS image sensor
Pixel detector
Tower Jazz
0.18um CMOS process

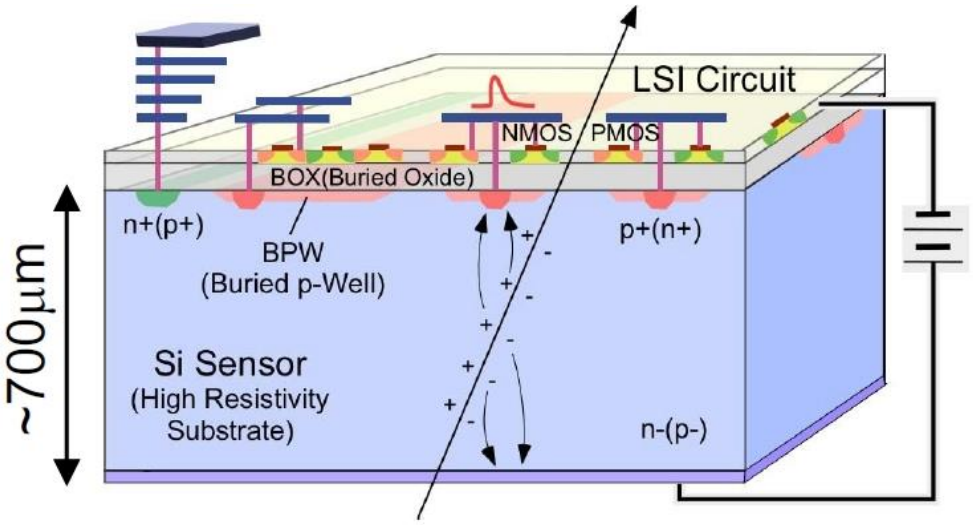
Advanced detector

Lapis Semiconductor
0.2um SOI pixel process

X-ray detector, Vertex detector

Comparison of Bulk and SOI CMOS





Monolithic Bulk CMOS pixel detector
Commercial processes
Only 1 active Si layer
Well structures
(cause larger pixel size)
Low material budget
Partial depletion (thin sensor layer)

Monolithic SOI pixel detector
Commercial SOI pixel process
2(or3) active Si layers
Well structure is not required
(small pixel size)
Low material budget (after thinning)
Full depletion (sensor layer < 725um)

Collaboration activity

KEK → IPHC

Researcher visited
Reported activity
- SOI sensor design
- 3D integration
- PDD structure

IPHC → KEK

Researcher visited
Reported activity
-Digital circuit design
-Digital circuit library
Design SOI digital library and participate MPW run

Report in Japan (KEK)

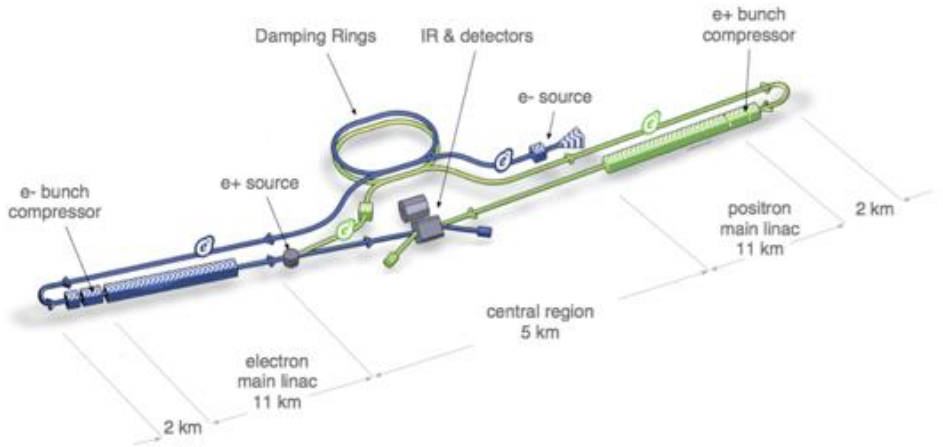
Sensor development SOFIST ver.3 and ver.4

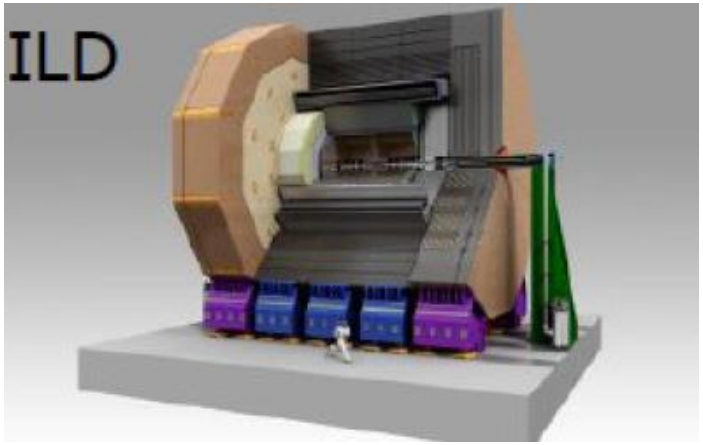
Exchange information on SOI technology and CMOS digital library:
Key1&2

International linear collider (ILC)

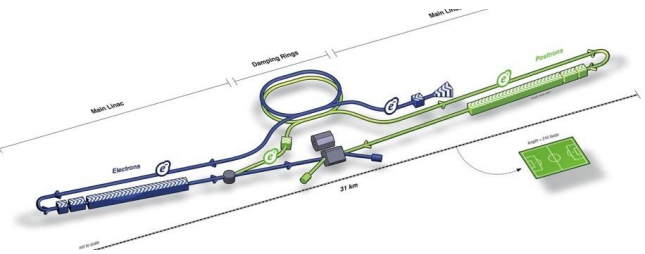
Requirement
Of vertex detector

Single point resolution: < 3 um
Small pixel size: < 25um pitch
Occupancy resolution: 554ns interval
Bunch identification during beam train
Low material budget: ~ 0.1 % /X0
Corresponds to ~ 100um Si thickness
Low power consumption: 50mW/cm^2 + gas flow cooling
Radiation hardness: TID 1kGy/year
NIEL 10^11 1MeVNeq/cm2/year





e+ e-
Center of mass energy: 250 GeV



SOFIST

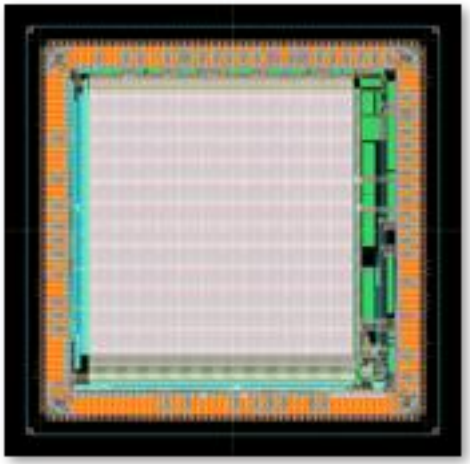
(SOI sensor for FIne measurement of Space & Time)

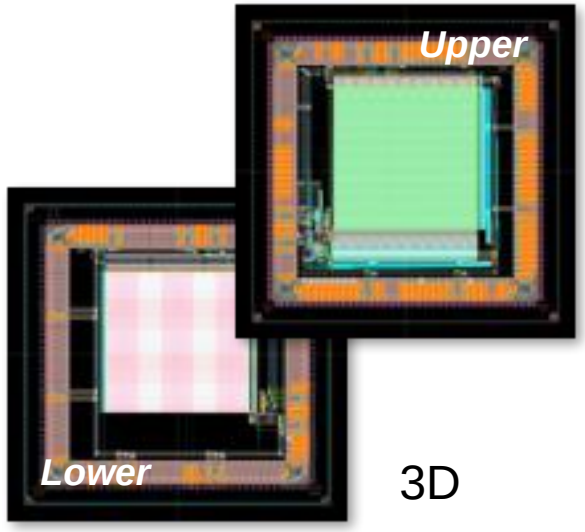
S. Ono, M. Yamada
(KEK)

Conceptual design of SOI pixel sensor
for the ILC vertex detector

Goal:
Single point resolution < 3um
Pixel size 20-25 um pitch
Time resolution >~ 554ns
In-pixel timestamp circuit

2D





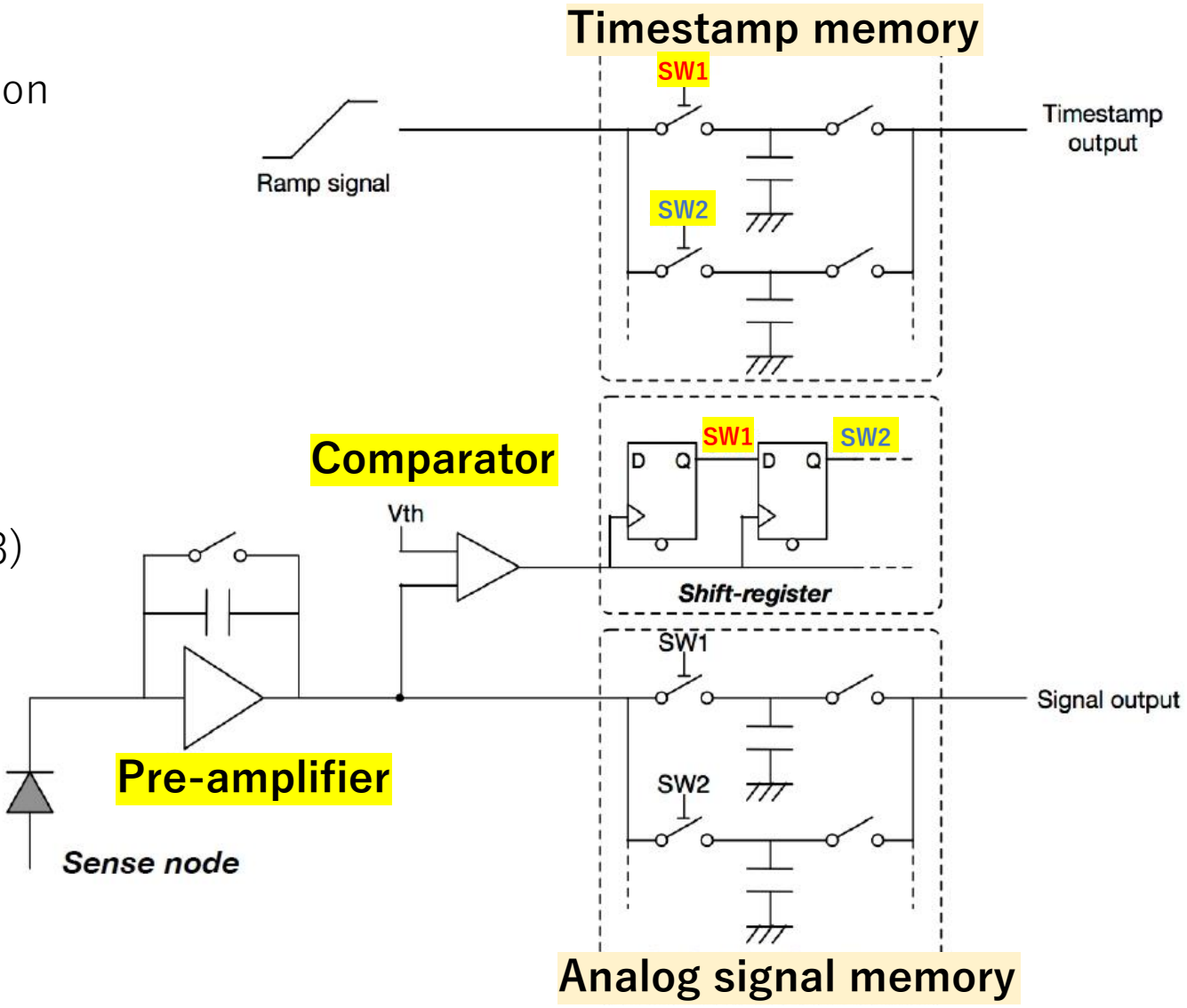
3D

	Ver. 3 (2D)	Ver. 4 (3D)
Chip Size	6mm x 6mm	4.45mm x 4.45mm
Pixel Size	30um x 30um	20um x 20um
Pixel Array	128 x 128	104 x 104
Circuits	CSA + Comp.+ 3 Analog Mem + 3 Time Stamp Mem	
Wafer	FZ p-type (3~10 kΩ·cm) Double SOI	

SOFIST (ver.3 and 4) pixel circuit

Pre-amplifier
Comparator
Hit-signal discrimination
Shift register
Latch hit signal

Multiple memories:
Analog memory(3)
Store charge signal
Calculate weighted canter of charges
Timestamp memory(3)
Store hit timing



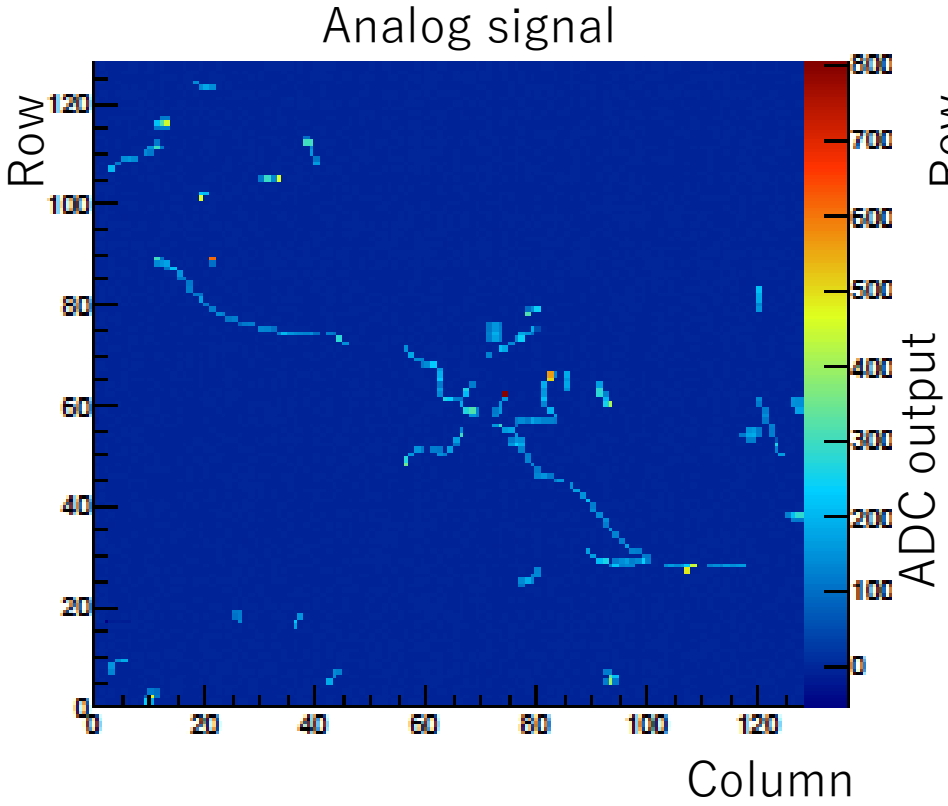
Position and Time Measurement

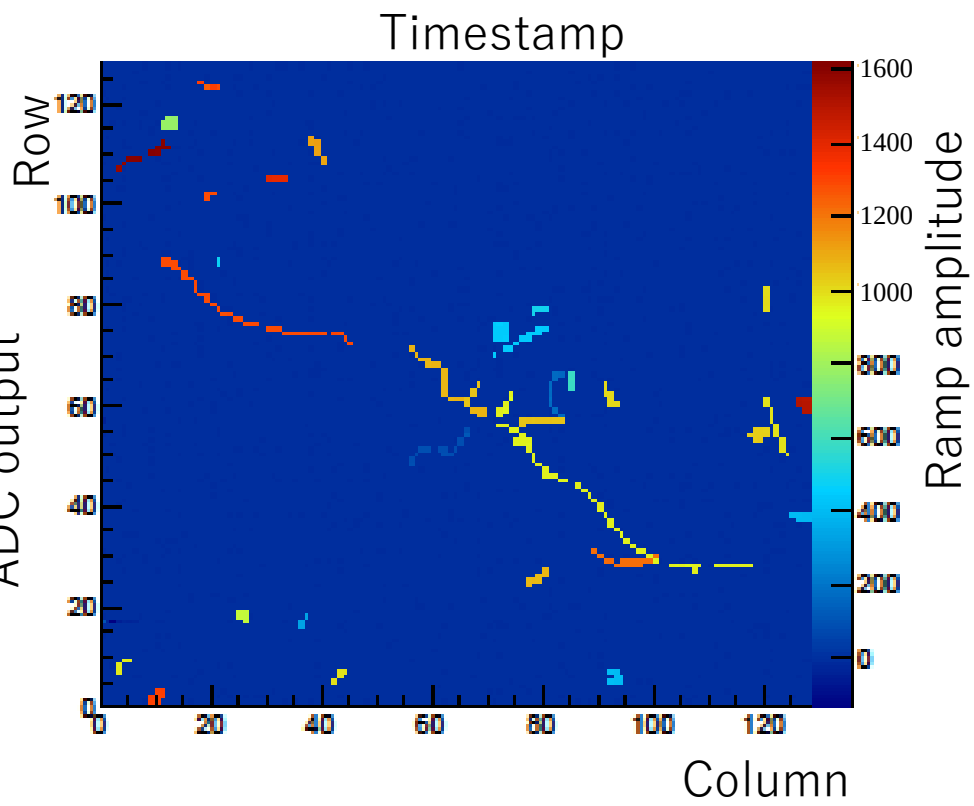
SOFIST Ver. 3

β –ray track from ^{90}Sr

Threshold: V_{th} = 910 mV, V_{RST} = 900 mV
HV = -100 V

* Pedestal subtracted





Measure signal amplitude and time in a pixel

120 GeV proton beam test was done on Feb. 2019 and under analyzing data (at FermiLab)

3D stacking (T-micro)

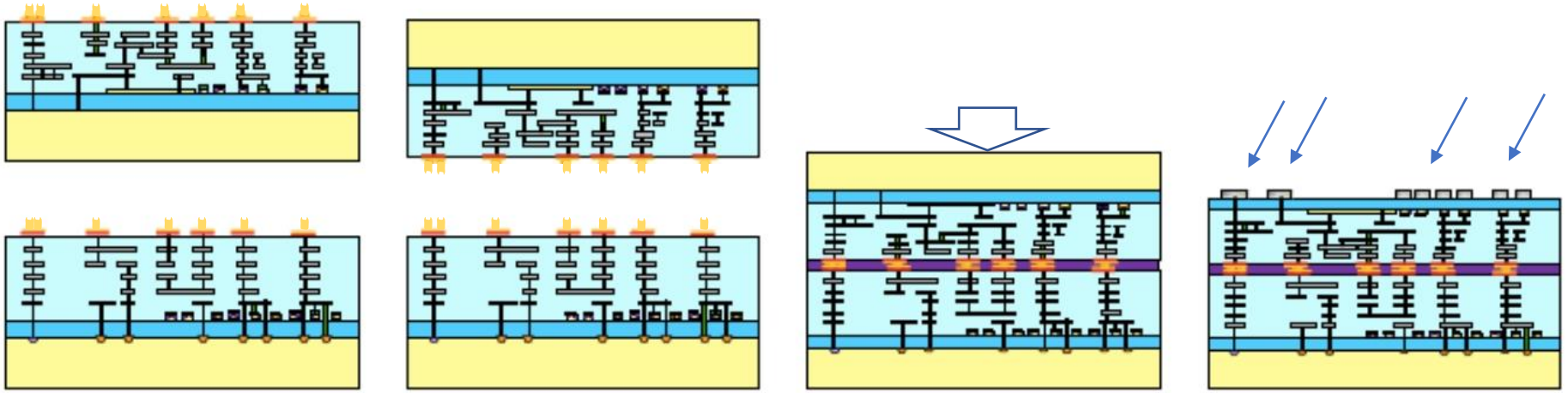
1. Form bumps

2. Stack and press

3. Remove upper substrate

4. Form IO pads

“Upper” chip

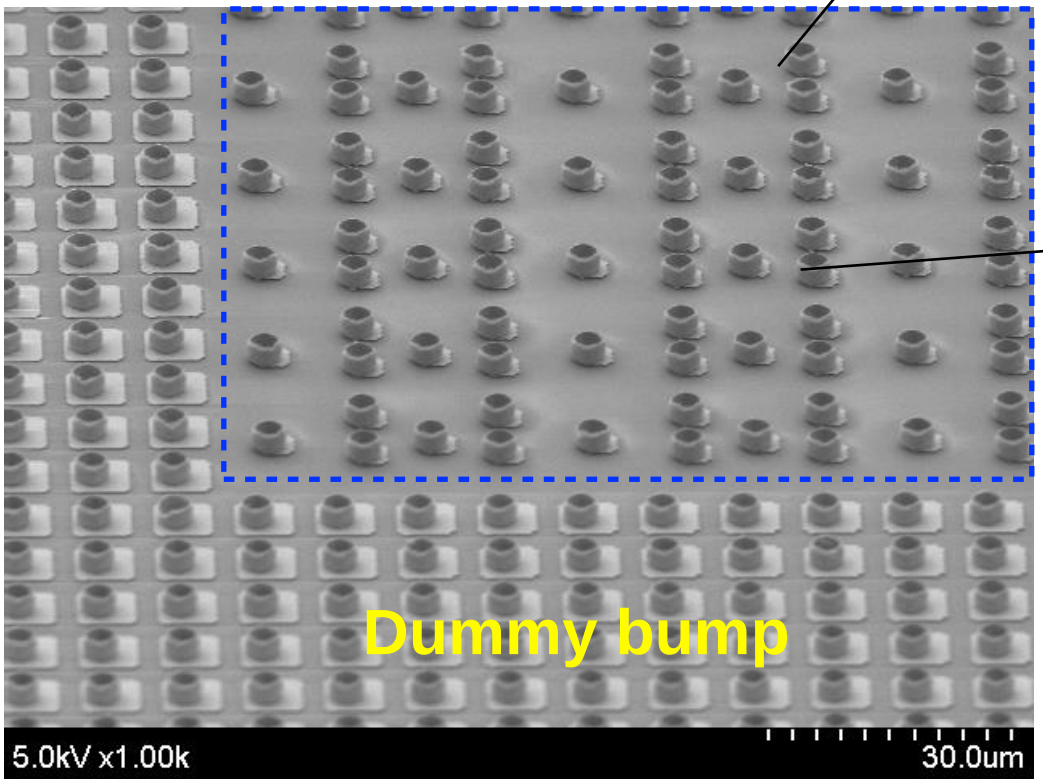


“Lower” chip

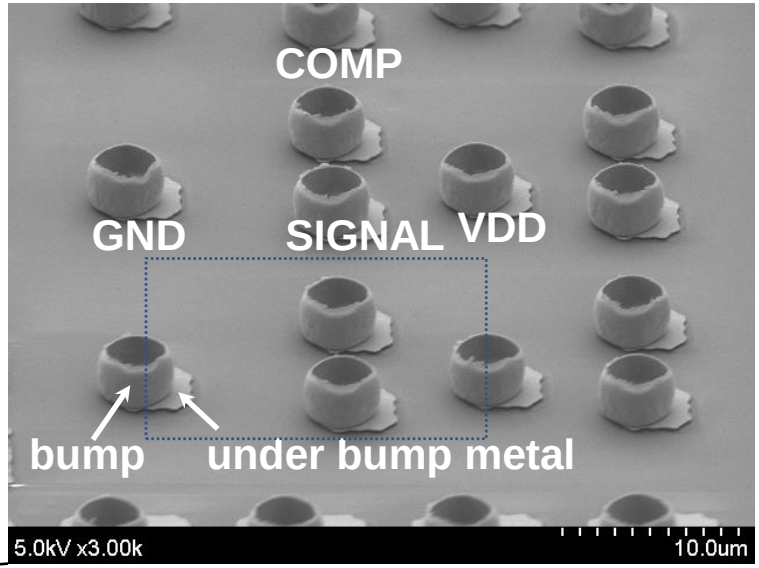
SOFIST Ver.4 Bump

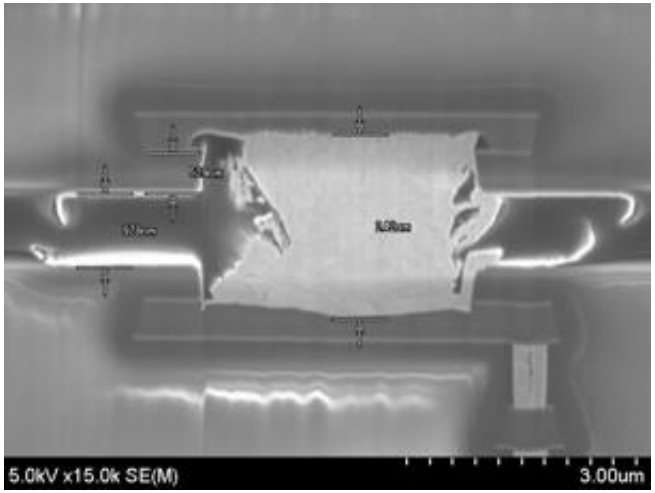
Cylinder bumps are successfully fabricated

Pixel array



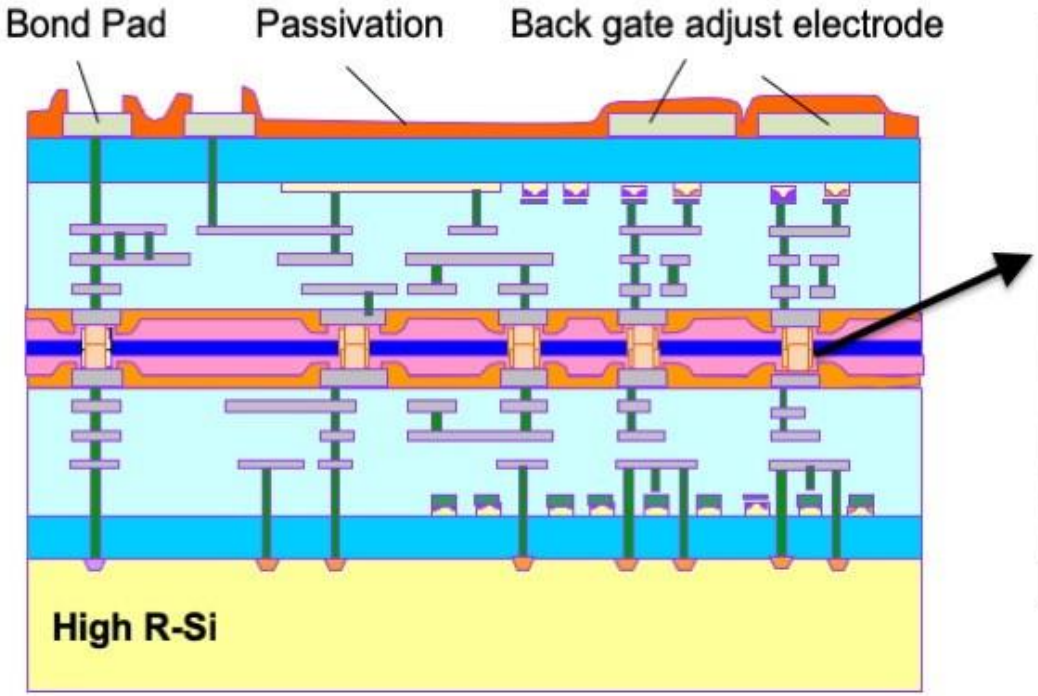
Pixel (20um sq.)

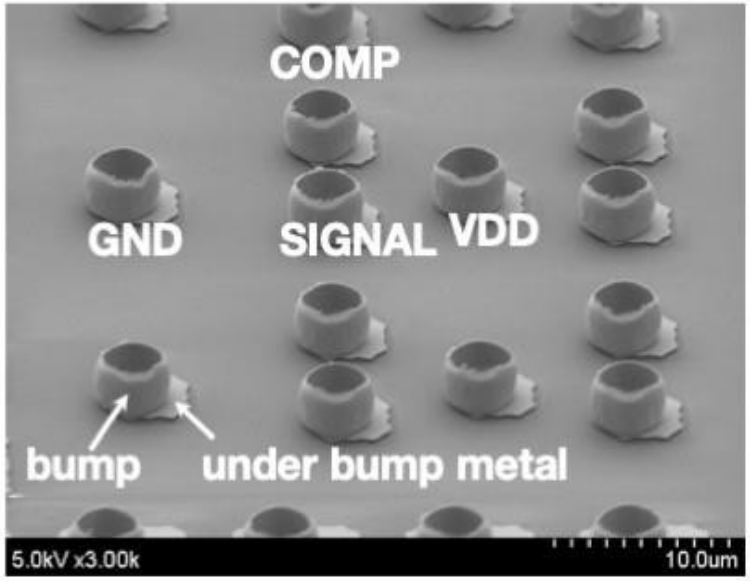




Sliced view at bump

Fabrication status of SOFIST ver.4



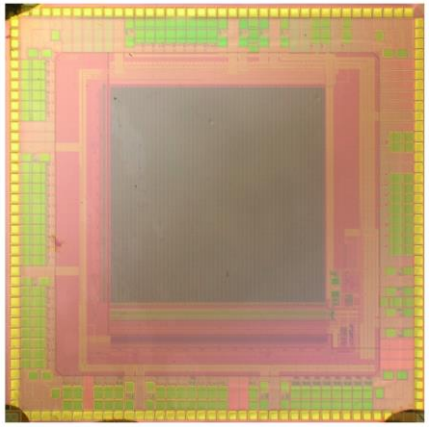


3D integration scheme of SOI chips.

Cylinder bumps fabricated in the pixel area.

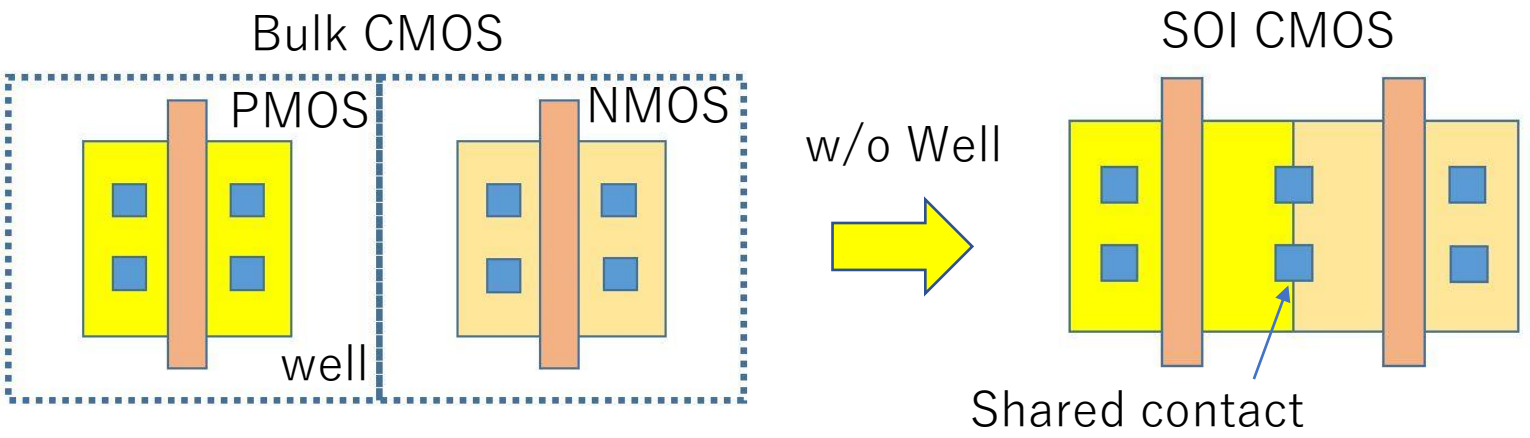
First chip was delivered in the end of FY2018

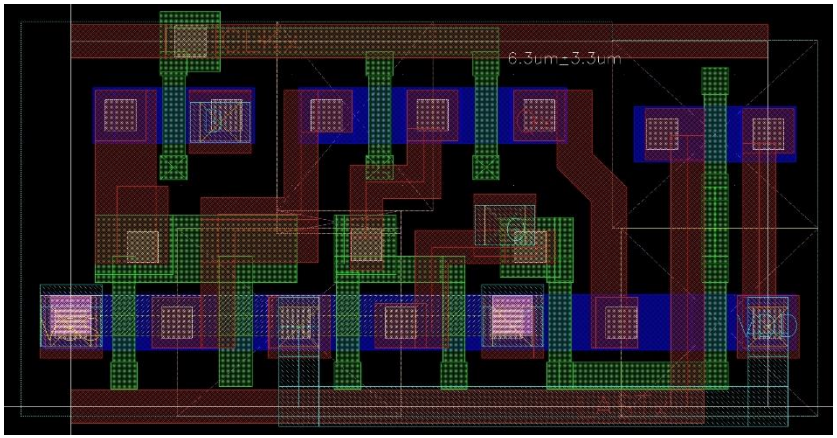
Under testing



SOFIST ver.4 bump-bonded chip

Key1: Active marge method in SOI-CMOS

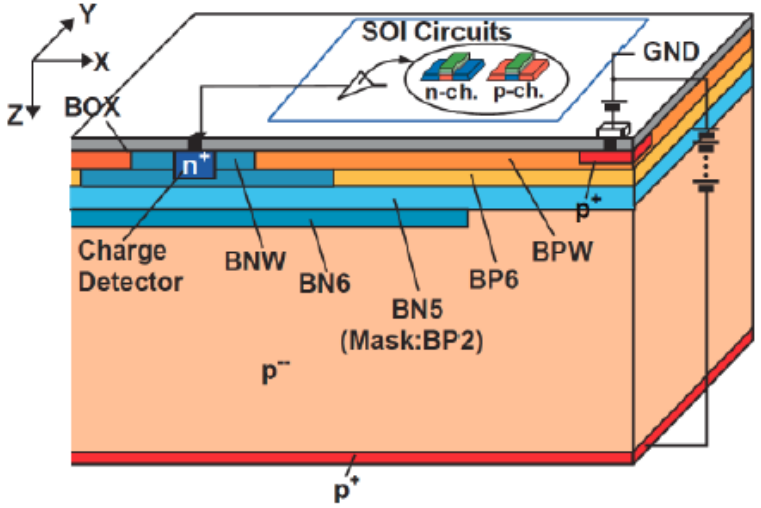




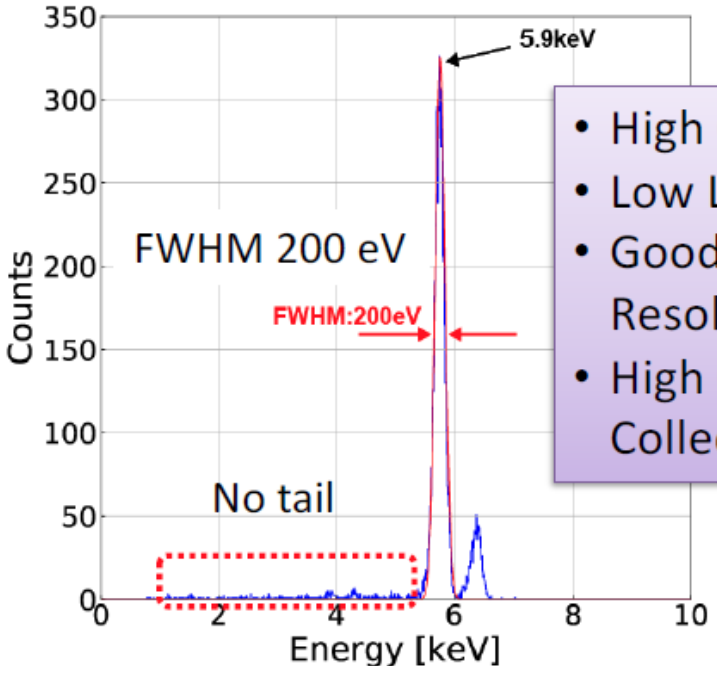
(Ex.) D-flip flop circuit with “active marge” method
(6.3um x 3.3um)

Key2: Pinned Depleted Diode (PDD) Structure

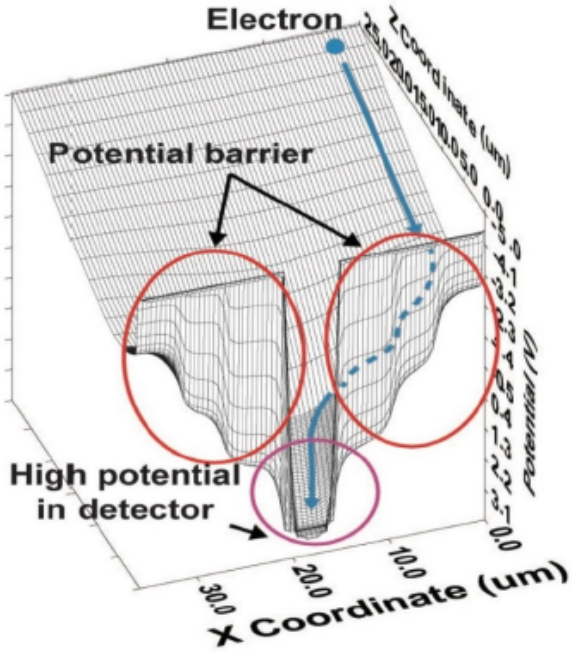
Shizuoka U. : S. Kawahito et al.



Gain = 70 μV/e-
Noise = 11.0 e-
Dark Current = 57 pA/cm2 @-35˚C



- High Gain
- Low Leak Current
- Good Energy Resolution
- High Charge Collection Efficiency



55-Fe measurement

Simulation

Report in France (IPHC)

First submission of chips on SOI technology

Report from Maciej Kachel (IPHC/IN2P3)

PICSEL group first SOI prototypes

- Context:
  - Current main IPHC project: MIMOSIS sensor for CBM experiment
    - 180 nm CMOS process over thin epitaxial layer (25 µm)
    - Good spatial resolution (5 µm) but better (≤3 µm) is required for ILC

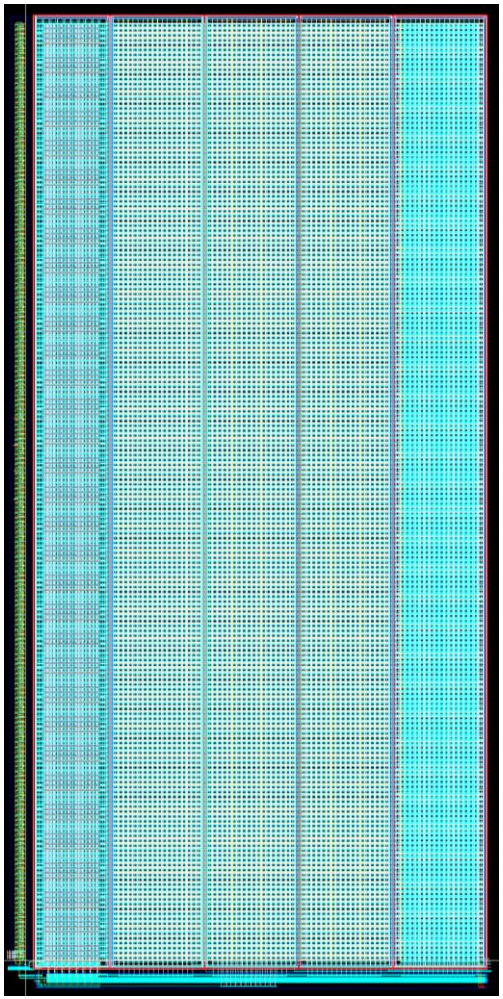
  → Investigate solutions in CMOS process & SOI technology

- Three test chips submitted in SOI technology:
  - Sensor1: HEP application
    - To compare with known pixels in current CMOS process used at IPHC
  - Sensor2: X-ray analogue imager
  - Chip3: New Digital library test=> future needs

- Two versions of circuits will be provided by the foundry:
  - Thinned down to 50 µm => for HEP applications
  - with a thick bulk => for X-ray detection

Sensor 1: HEP applications

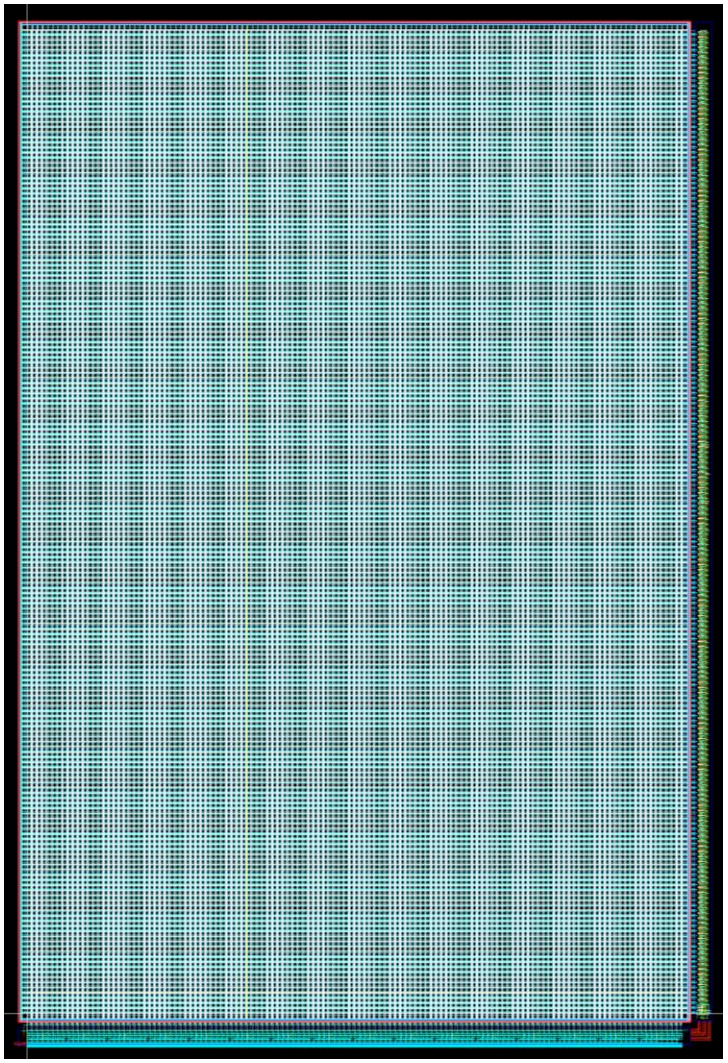
- Different pixel architectures:
  - Pixels with 18µm pitch
  - Sensing element : PDD
  - Pixels with various collecting diode structures
  - Various amplifiers:
    - MIMOSIS replica
    - New architecture (Sz. Bugiel AGH)



- Study:
  - Charge collection as driver of
    → detection efficiency
    → spatial resolution
    → Timing performance
    → Radiation tolerance

Sensor 2: analogue imager

- Architecture
  - Matrix of 128x192 pixels
  - 18µm pitch
  - Sensor: PDD structure
  - Rolling/global shutter

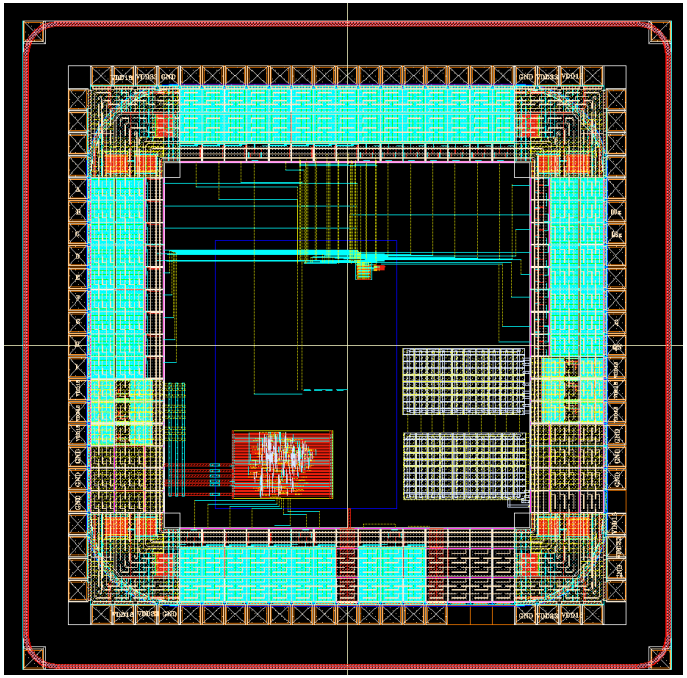


- Study:
  - Energy resolution
  - Spatial resolution
  - Quantum efficiency

- Applications:
  - X-ray spectroscopy
  - Electron imaging

Chip 3: digital library

- IPHC-KEK common development
  - M.Kachel(IPHC) and S. Ono (KEK)
  - Cells use the active merge to minimize area
    → Crucial for small & smart pixels



- Test chip contains:
  - Matrix of all of the digital cells
  - First synthesized block

→ Extracted timing performance of the digital cells will provide information on the development of the final SOI digital library

Summary

Progress

Japan: SOI sensors for future collider have been developed and evaluated. (SOFIST ver.3(2d) and ver.4(3d))

Japan & France : exchange researchers and share information on SOI-CMOS structure and standard CMOS digital library

France: First submission in KEK MPW run was done

Future plan

- Evaluate CMOS and SOI sensors submitted FY2018
- Review FY2018 design and discuss future submission
- Exchange researchers (seminars and meetings)
- Collaboration meeting