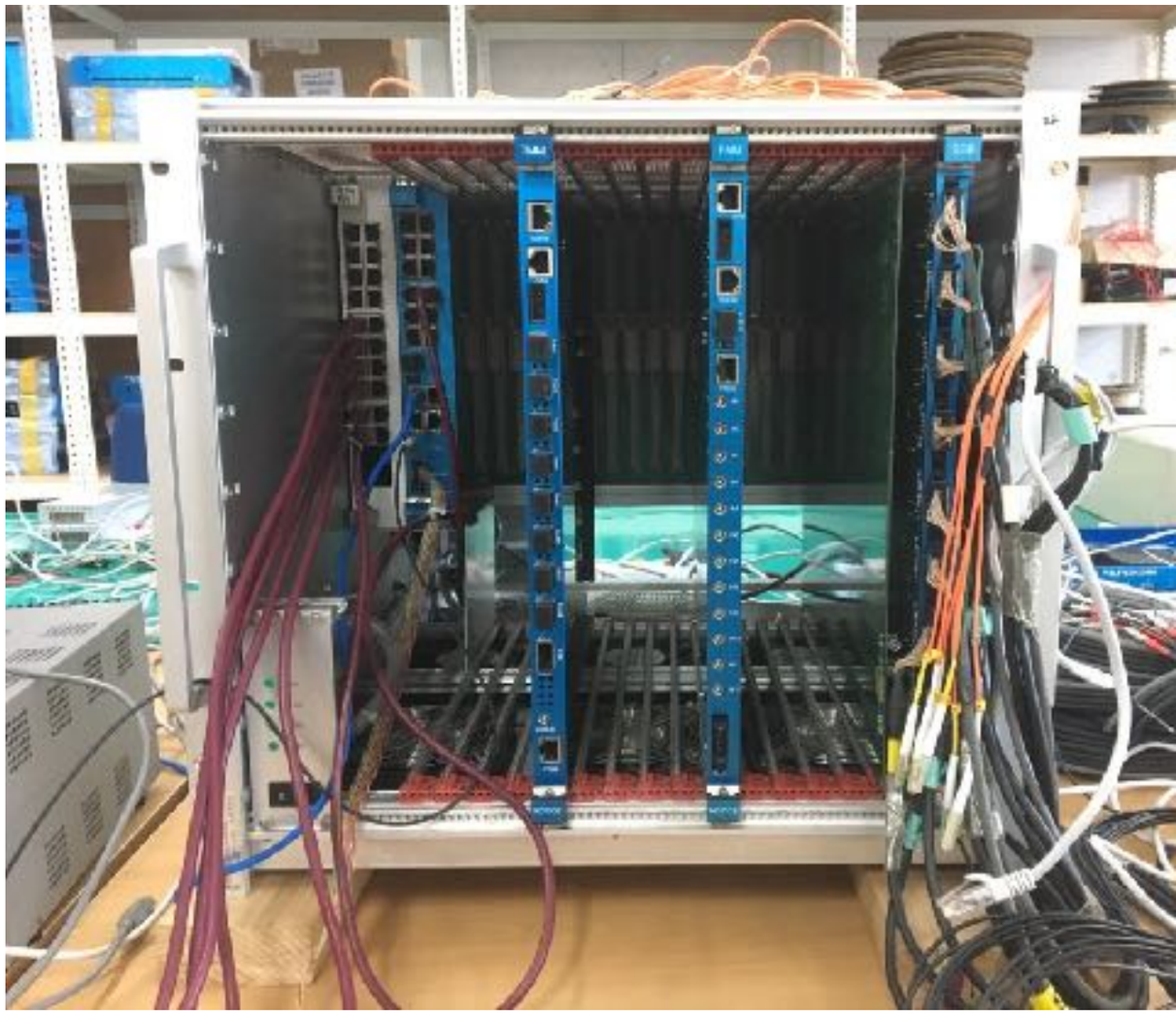
LAMPS DAQ 개발 상황

이종원

LAMPS DAQ electronics

- Board size : VME 9U 1 slot
- Interface : USB3/Optical link
- Power supply : Customized 9U VME crate.

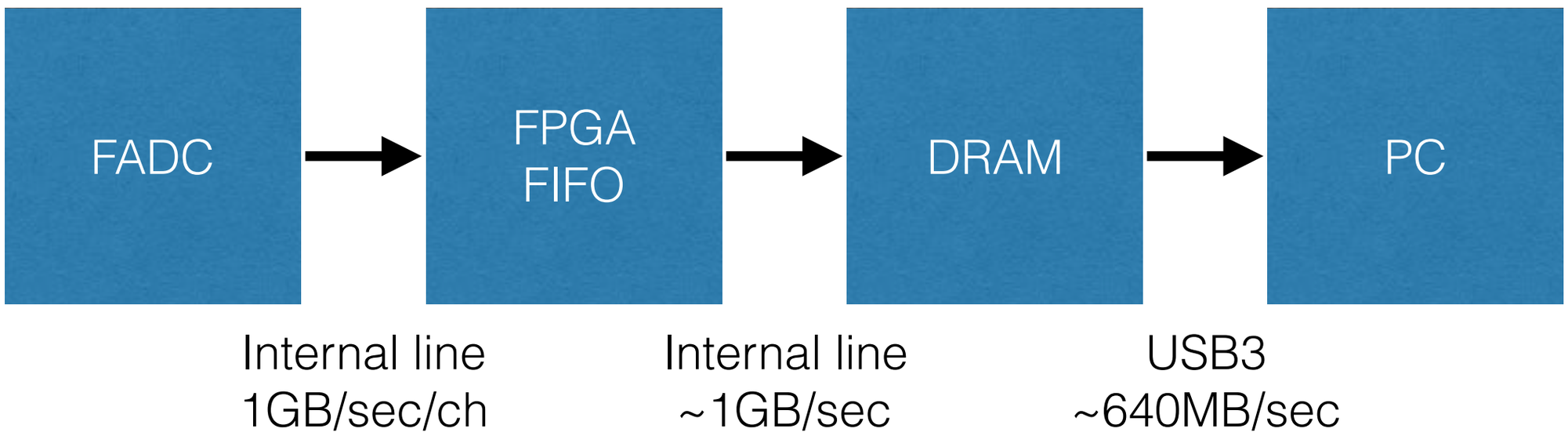
"Example view"



FADC Development status (Notice)

- Test Board : will be done in March
- a single revision will be available
- After an instrument test in KU, Notice will produce 100 channels for LAMPS.
- Period : within 1 month from KU test.
- Current status(3/6)
  - Under drawing the circuit schematics.
  - layout drawing will be started soon.

Structure of FADC



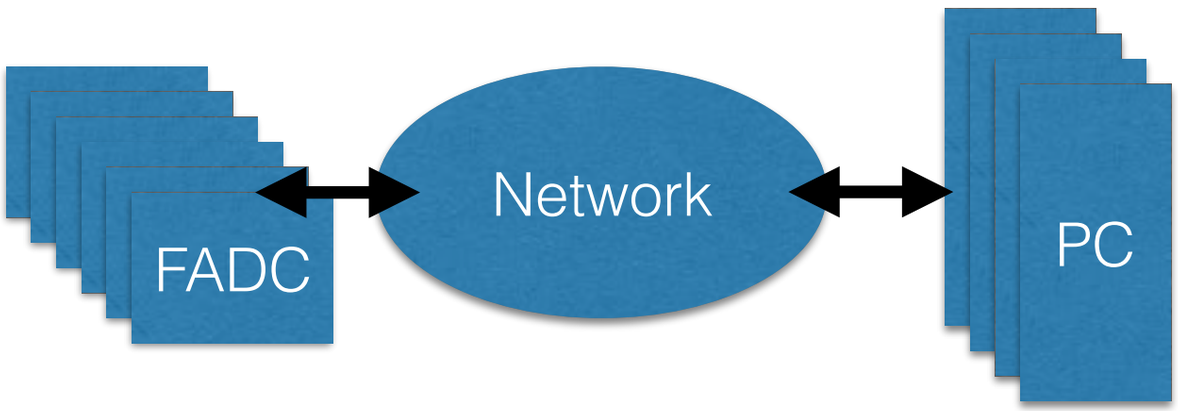
- FPGA FIFO size : 64kB x 4 (~64us with 500 MHz)
- DRAM readout size : 8kB per channel.
- If the next FIFO memory was not cleared, the FADC data will not filled into the FIFO.

Requests/Advices from Notice korea

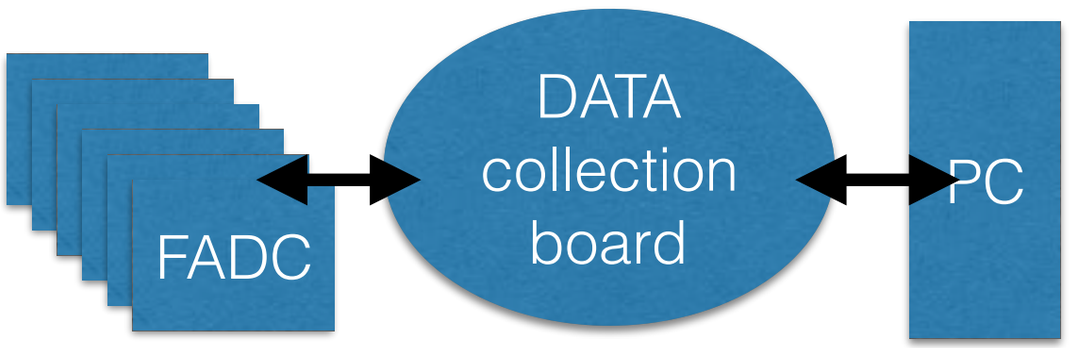
- The specification of optical links for FADC is 5Gb/s
- 1 optical link / 4 channel, = 2 optical link / 1 board
- In case of 100 channel,
  - -> 25 optical fiber modules are required
- For the connection, NO TCP/IP standard for 5Gb/s speed
- 10Gb/s optical link module is expensive.

Suggestion from Notice korea

- Make additional module, which collects data using optical link and communicates with PC
- Direct connection using optical link is not recommended.
  - driver for 5Gb/s optical link is required or using 10Gb/s optical link(expensive…)
- Many PC is required for a Neutron detector stage.



High cost, complicate
High speed



Low cost, simple structure
limited speed