# LAMPS neutron detector RCNP N0 beam test

이 종원

# Shipping Schedule



4/29 1차견적 170만/편도



5/11 CARNET신청



5/17 CARNET 접수 (산단에서 5일 지체)



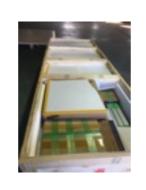
5/26 RCNP 도착(2일 지연)

4/15 운송업체 접촉

#### 5/9 INVOICE



#### 5/12 운송회사위탁



## /일본수출



5/19 CARNET 발행 6/9 고려대도착 총 비용 : 140/편도 511Kg / 1.943 CBM

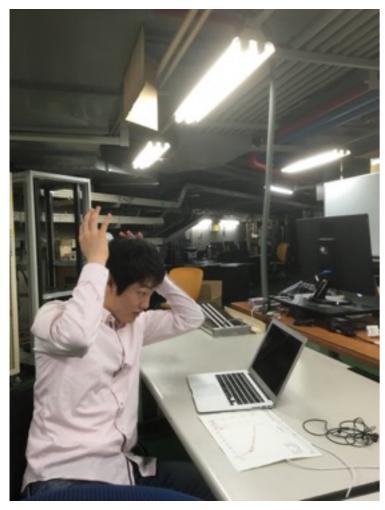


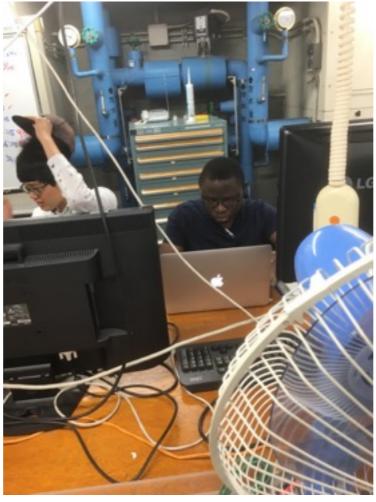




### Beam test Time table

- 1. 5/24-25: Checking area & cable preparation
- 2. 5/26-27:Unpacking luggage, building support structure, detector preparation
- 3. 5/28:Cosmic ray data for calibration
- 4. 5/29: Change setups for beam test and cosmic ray data taking
- 5. 5/30: 10AM-5PM Al target test. 394MeV (18 run )
- 6. 5/30: 5PM-12PM Li target 394MeV (50 run)
- 7. 5/31: 2AM-6AM Li target 65MeV (50 run )
- 8. 5/31-6/1: Disassemble setup, packing









Setup (downstream)

# Analysis Plan

Cosmic ray	Neutron Data(394) Neutron Data(65)	Waveform
Energy Calibration Hyunha	Electron-equivalent energy vs TOF neutron energy Hyunha	Time from Waveform Benard
Position Calibration Hyunha	T0 Calibration Hyunha	Height vs waveform Benard
Timing resolution (cosmic ray): Hyunha	Time-information correction Hyunha	Particle vs waveform Benard, Lee
Position resolution (cosmic ray): Hyunha	G4 MC full simulation Hyunha	Waveform simulation Benard

# Hardware design plan - Support structure

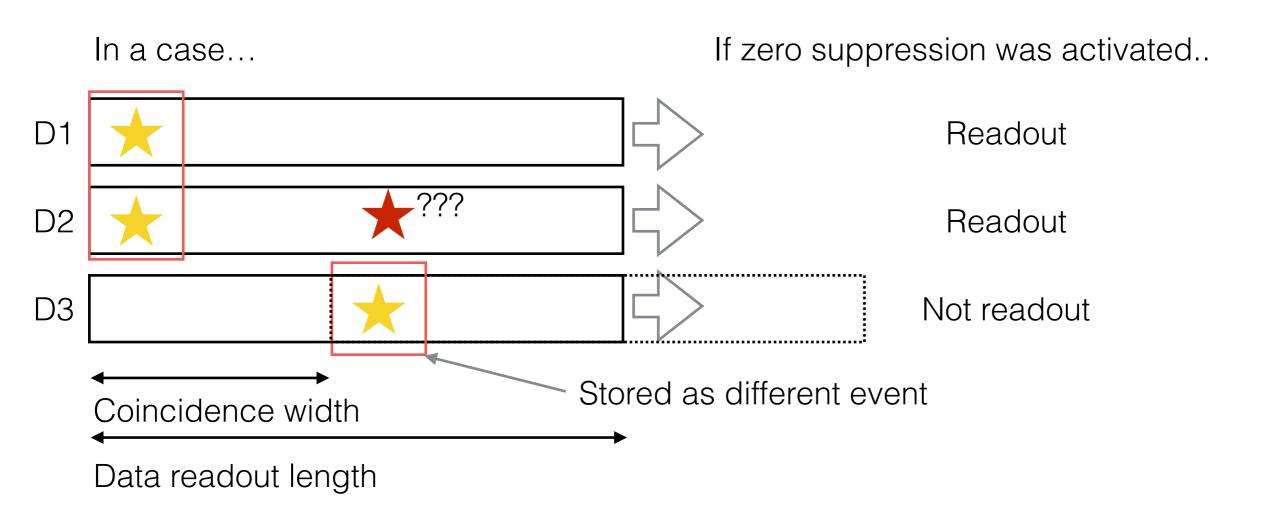
- 1. Currently stopped...
- 2. A student will start designing in August.
- 3. Gluing light guide and scintillator.
- 4. Supporting structure will be fixed at the detector.

# Known problems of FADC Electronics

- Ambiguity of trigger / Veto
- 2. Flushing Data partial data readout
- 3. Junk data readout
- 4. High rate problem
- 5. Protection circuit for FADC



# Ambiguity of trigger / Veto



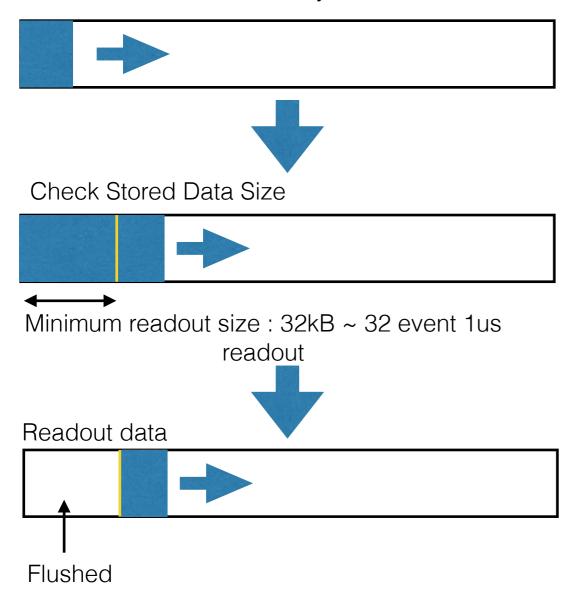


There are no VETO system to issue new trigger within data readout length.( in my opinion) -> They should be VETOed.

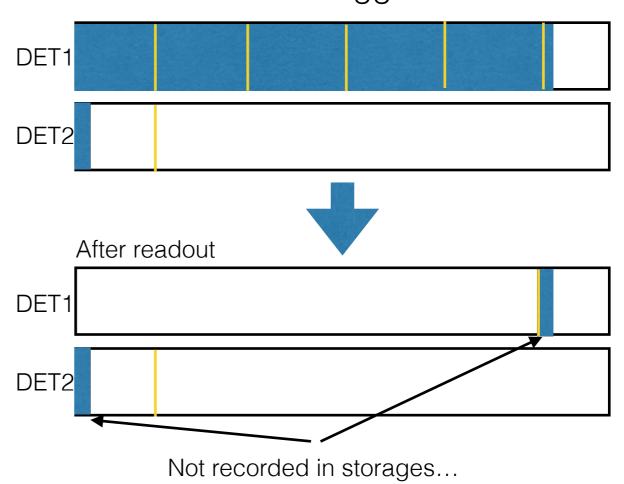
# Flushing data problem

#### Data readout mechanism

Maximum memory size: 4GB



If..: multiple detectors with extremely different trigger rate



If data acquisition was stopped before readout, data of detector 2 will not be recorded for the run....

=> Consider trigger rate / data readout speed

## Junk data readout

- 1. FADC refreshes memories when it initialised.
- 2. However, sometimes? memories dose not refreshed, and FADC readout junk region, binary data conversion fails.
- 3. Solution : change FADC initialise process.

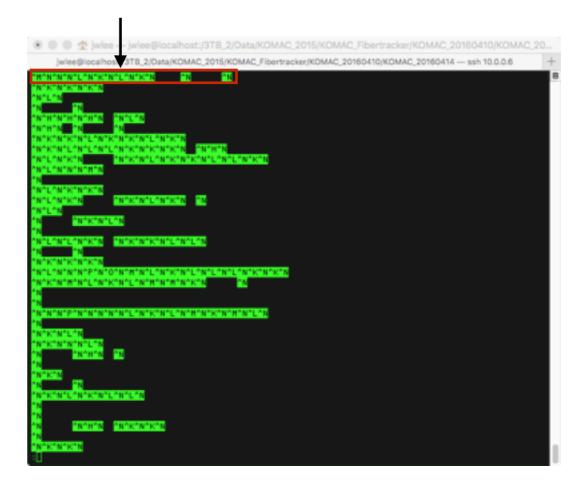
## Common

#### Header(32 char)



#### Junk Data

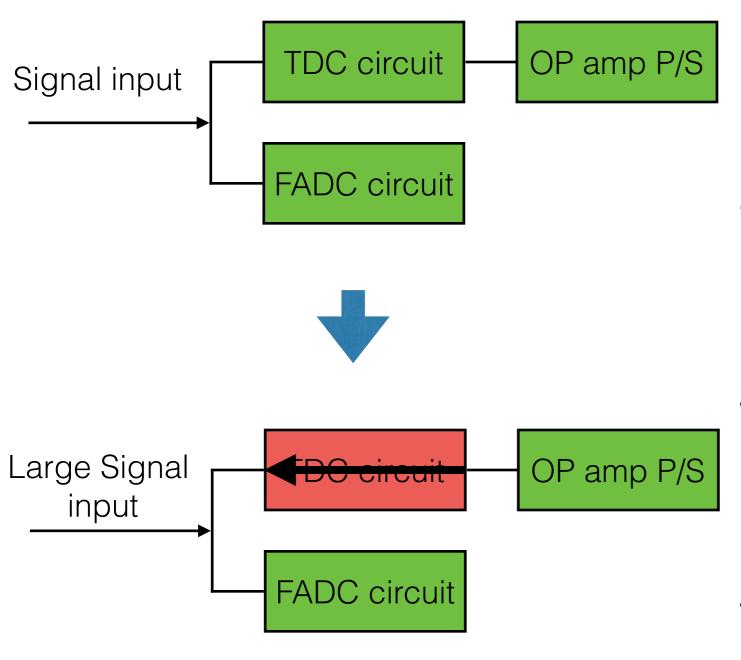
#### No Header



# High rate problem

- 1. FADC electronics endures up to 500kHz trigger rate. (for single channel)
- 2. Problem is...
  - Readout speed via USB3 cannot support maximum recording speed of FADC internal memory.
  - 2. No signal/VETO system when the internal memory is full.

## Protection circuit for FADC



- Large signal input -> destroy OP amp for TDC
- 2. The OP amp circuit break down and power line and signal line were connected.
- 3. A offset readout by FADC will be 0 -> not triggered by trigger setting.
- 4. Protection circuit is required.

# Future electronics plan

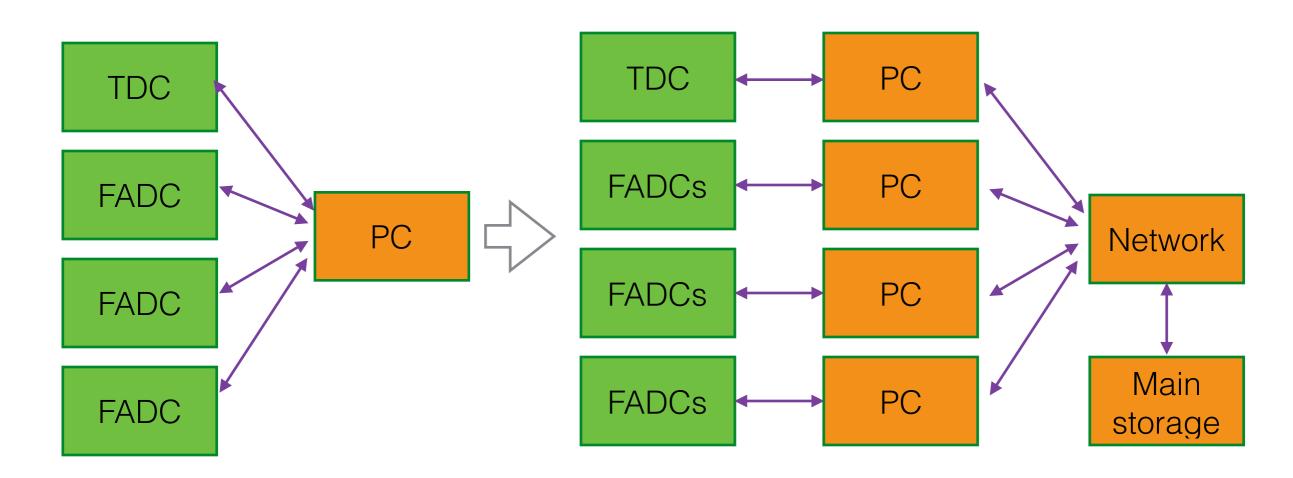
- DAQ development
  - 1. Integration with CAMAC / VME
  - 2. Readout data with multiple machine
  - 3. Semi-online event reconstruction

# Integration with CAMAC / VME

- For the beam test in Michigan Uiniv.
- Software/hardware development for matching event between FADC and CAMAC/VME system.
- DAQ will be developed with network programming for multiple DAQ PC.

# Readout data with multiple machine

- 1. Current DAQ program is developed for single machine.
- 2. If there are multiple FADC module, the writing speed of PC(SSD or HDD) will be limited data taking speed. + Physical limits on USB3 cable length.



# Semi-online event reconstruction/display

- 1. Currently, realtime event reconstruction is unavailable due to data store structure.
- 2.Only semi-online event reconstruction/display is available.
- 3. Bypass a part of data to independent machine and event reconstruction.

