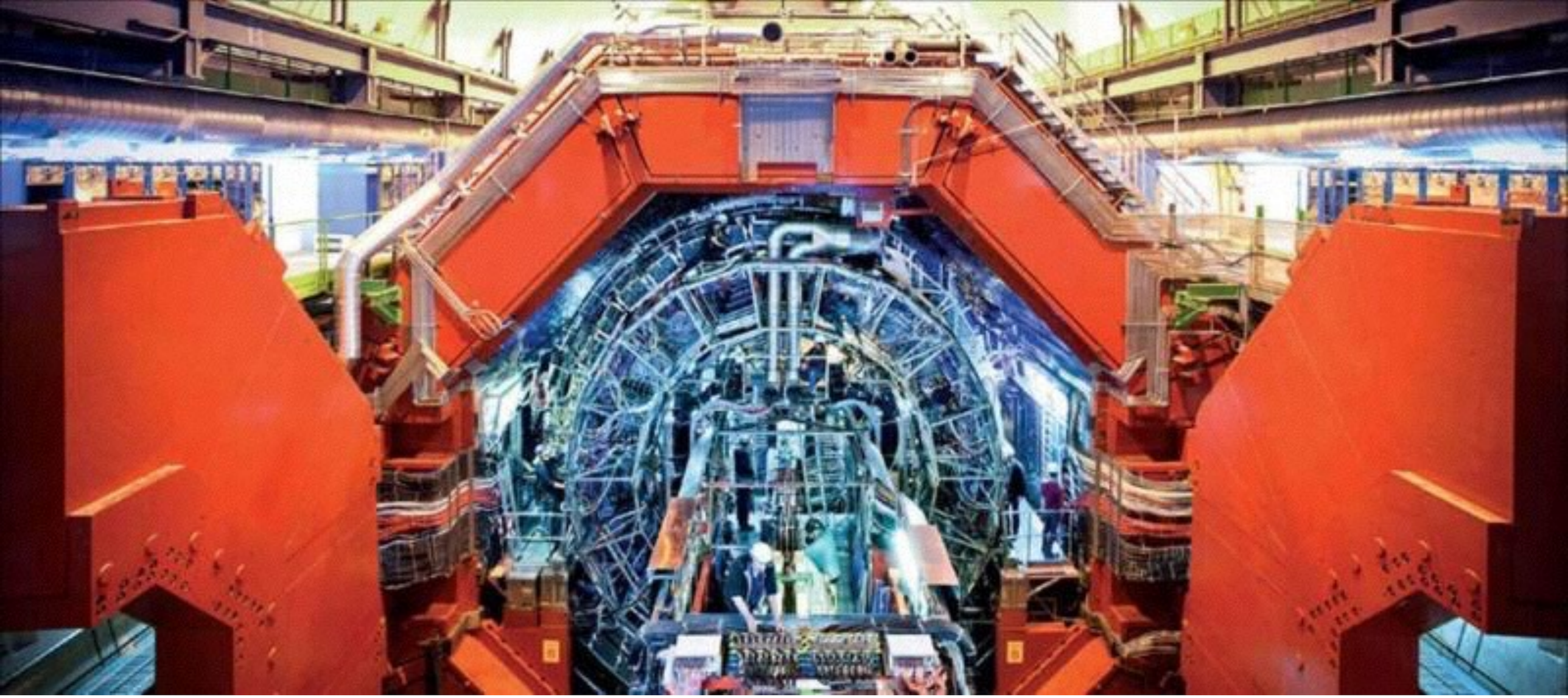

Studies for an upgrade of ALICE Inner Tracking System:

Pixel chip characterization

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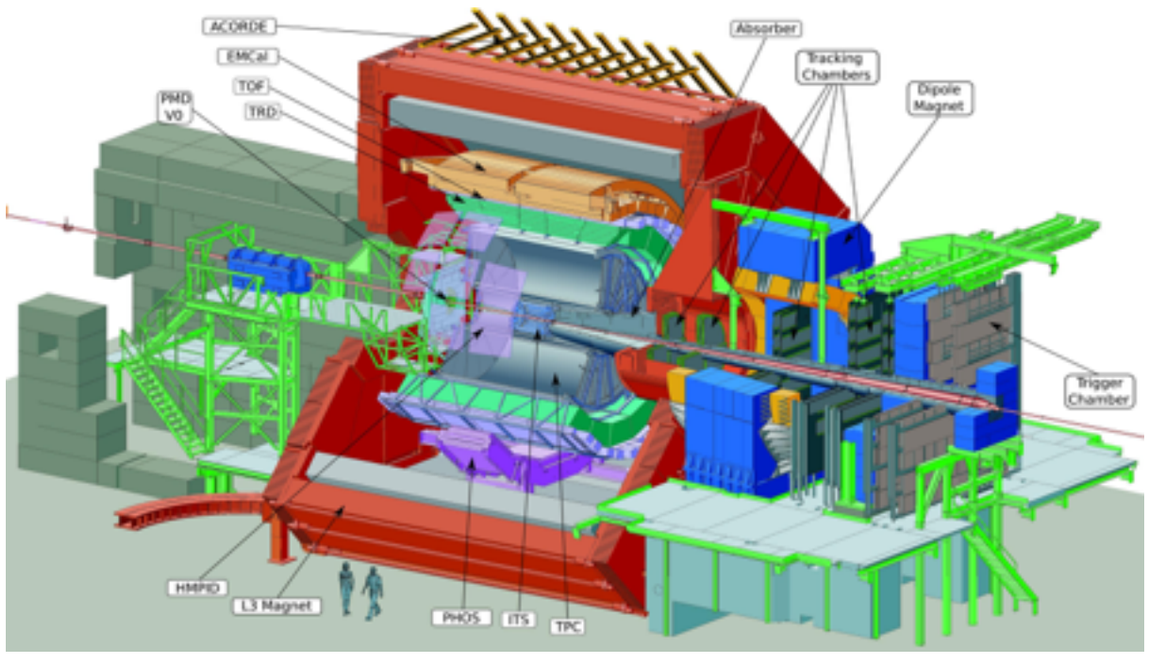
KAL hotel, 29 Aug 2016

ALICE

Physics motivation



A Large Ion Collider Experiment

- ALICE confirms basic picture by observation of hot hadronic matter at unprecedented values of temperatures, densities and volumes and exceeds the precision and kinematic reach of all significant probes of the QGP measured in the past decades
- Further progress on the characterization of QGP properties requires precision measurements of rare probes over a large kinematic range(from high to very transverse momenta) and as a function of multi-differential observables (centrality, reaction plane, …)

  One example: precision measurements of spectra, correlations and flow of heavy flavour hadrons and quarkonia at very low transverse momenta

  ➡ Requires statistics(luminosity) and precision measurements
- Required detector upgrade, especially inner tracking system

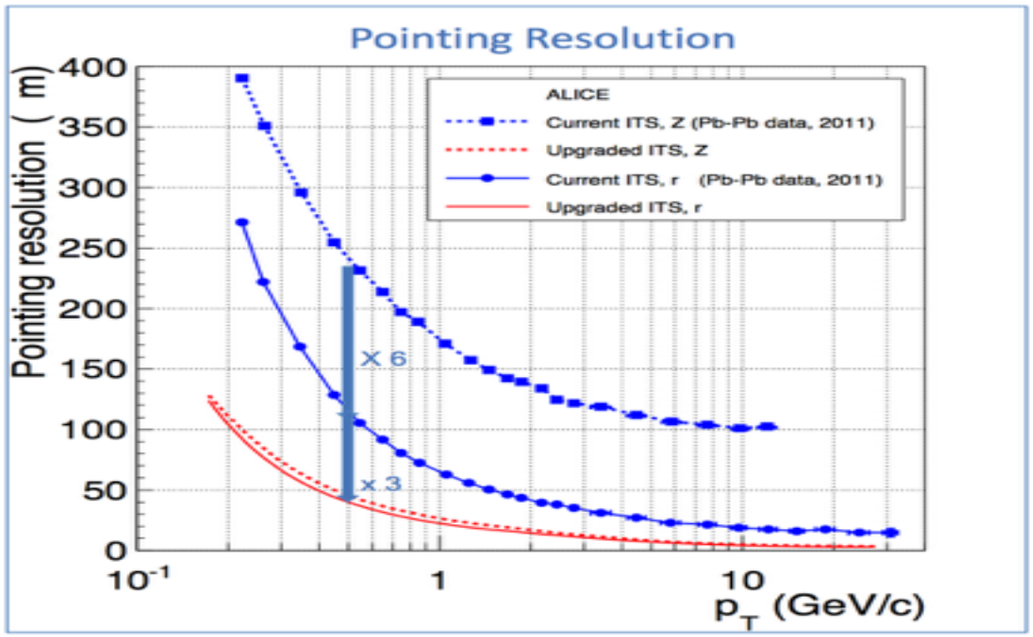
ITS upgrade design objectives

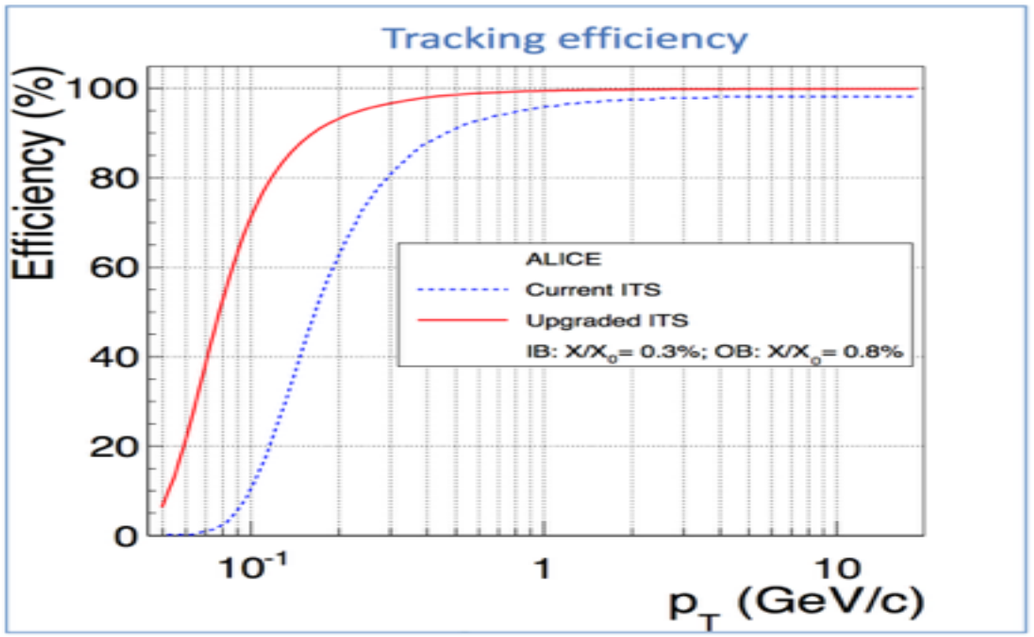
1. Improve impact parameter resolution by a factor of ~ 3
   - Get closer to interation point (position of first layer) : 39mm → 22mm
   - Reduce material budget : ~ 1.14% → ~ 0.3% (for inner layers)
   - Reduce pixel size : 50 μm x 425 μm → 30 μm x 30 μm

2. Improve tracking efficiency and p_T resolution at low p_T
   - Increase granularity : 6 layers → 7 layers, silicon drift and strip → pixel
   - Increase radial extension : 39 - 430 mm → 22 - 430(500) mm

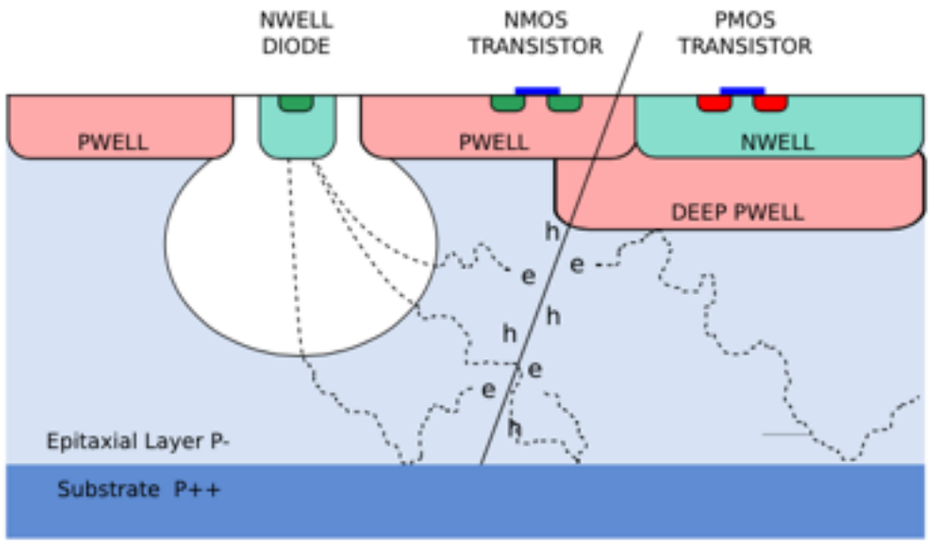
3. Fast readout
   - Pb-Pb : > 100kHz / p-p : ~ MHz

4. Fast insertion / removal for yearly maintenance
   - Possibility to replace non-functioning detector modules during yearly shutdown





Pixel chip technology



Tower Jazz 0.18µm CMOS

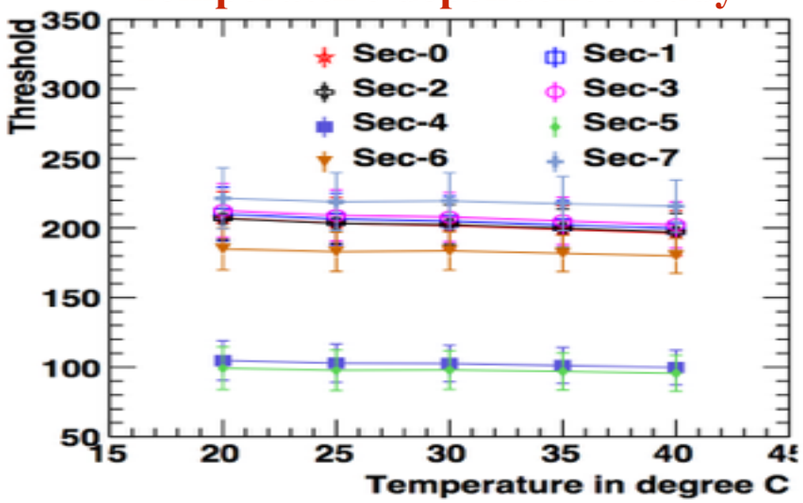
- feature size : 180 nm
- metal layers : 6
- gate oxide : 3nm (good for TID)

- Monolitic Active Pixel Sensor technology (MAPS)
- Deep PWELL shields NWELL containing PMOS transistor from collecting signal charge
  ➡ Allow for full CMOS circuitry whithin active area
- High-resistivity(>1kΩ cm) p-type expitaxial layer on p-pyte substrate
- Depletion region around NWELL collection diode increases with increasing reverse substrate bias

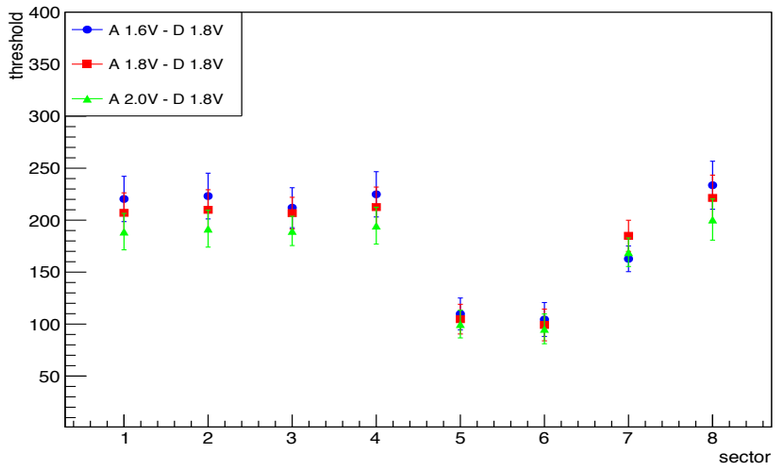
Test setup

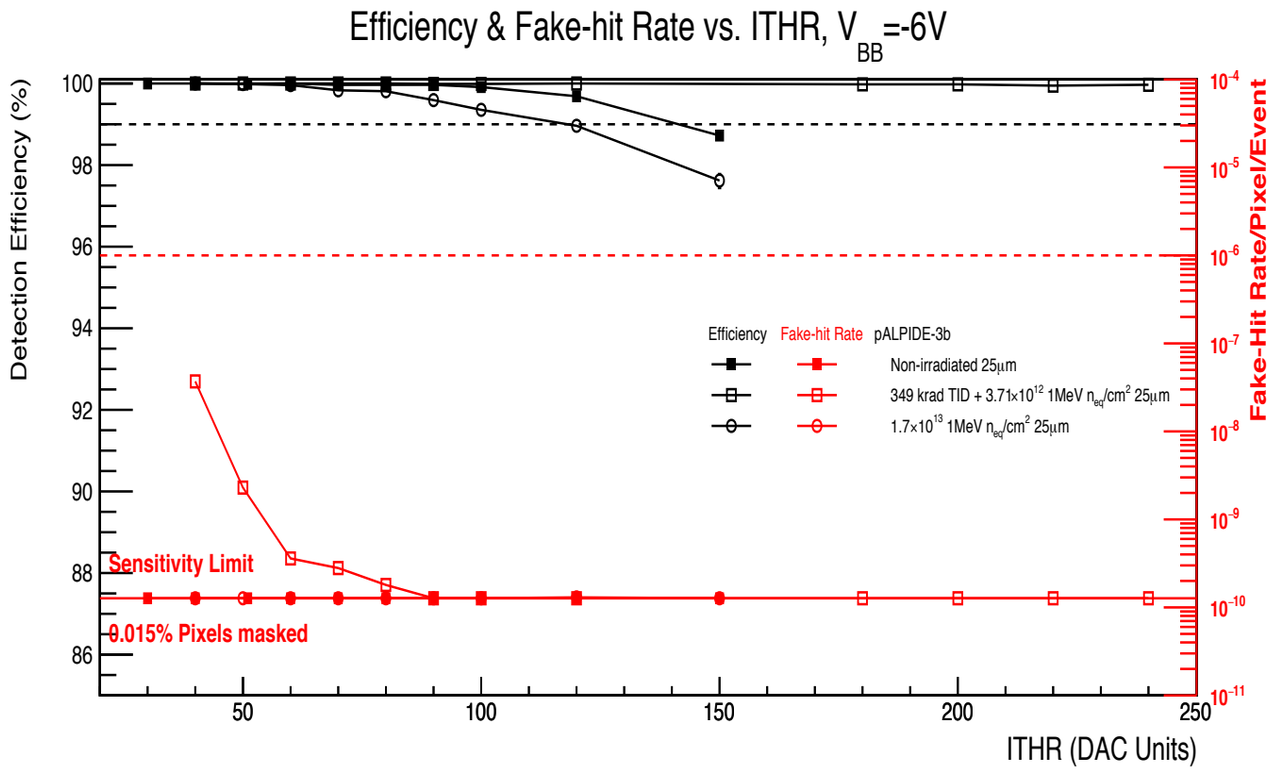
- USB-based Test system used both for lab measurements and test beam
- Lab. test: temperature dependence study, supply voltage dependence, noise injection study…
- Beam test: efficiency, position resolution, cluster analysis…

Temperature dependence study



Supply voltage dependence study





Summary

- For significant improvement of vertexing and tracking capabilities at low p_T, ALICE ITS upgrade is underway.
- The chip used in new ITS is developed in various phases by chip characterization test
- Chip characterization test has been performed in two parts : laboratory test, beam test
- The design goal of the chip is achieved from all characterization tests
- ALPIDE which is the final version of the chip has been commissioned on the basic of characterization test and has been producing