TPC Readout Electronics

Jung Keun Ahn
(Pusan)

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Requirements for LAMPS-TPC

- High-rate capability
- Large dynamic range
- Compact data size

High-Rate Capability

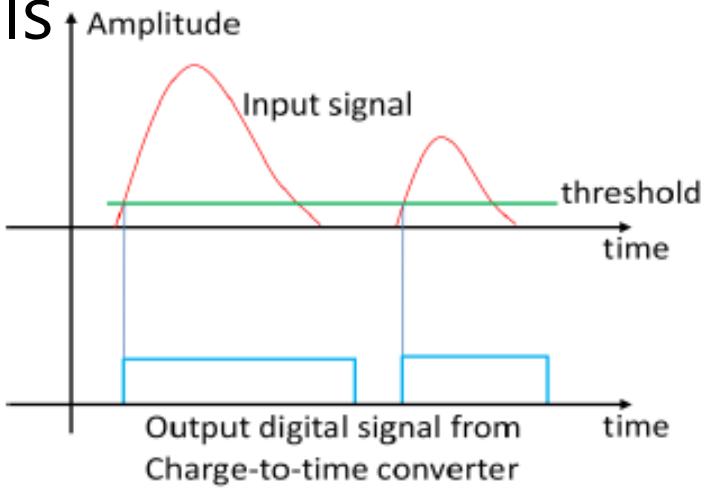
- Event rate
  - Beam and target nuclei
  - Beam current, target thickness
  - Collision rate
  - Requirements from Physics
- Drift velocity (Maximum drift time)
  - Multiplicity
  - Gas choice, electric field, pressure
- Trigger latency

Large Dynamic Range

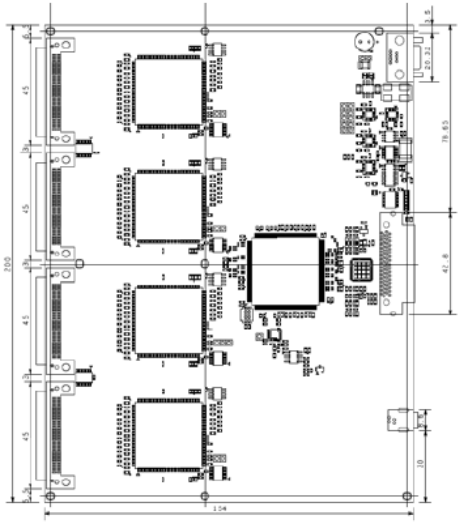
- Particle identification ($dE/dx \sim 1/\beta^2$)
  - e-e+ from $\pi 0 \rightarrow 2\gamma$
  - π and p
  - light ions
  - heavier nuclear fragments
- Good linearity in wide dynamic range

Compact Data Size

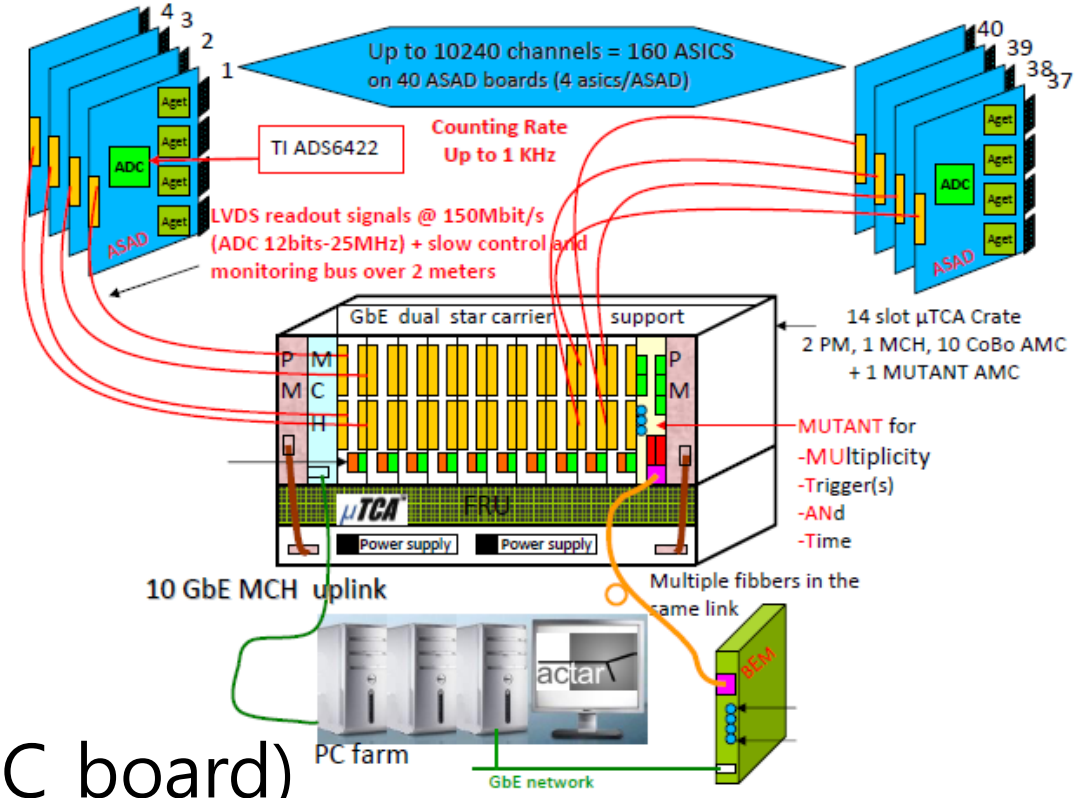
- Deadtimeless data-taking
- Charge and time measurements
  - Pulse shape information
  - 10-bit, 12-bit, 14-bit in ADC
- Flash-ADC, TDC or others
- Number of readout channels
- Zero suppression
- 10-100Mbps?



GET scheme



200x154mm



- AsAd (ASIC and ADC board)
  - 256 ch / board, 4 AGETs, 12-bit ADCs
- CoBo (Coordination board)
  - Zero suppression, Network transfer to PCs
- MUTANT-BEM (Trigger)

Cost estimates for the GET system (1)

- A single production batch of 800 AGET chips costs 20M JPY (300 M KRW).
- A production yield is expected to be 80%, so we will have 640 chips or 640 x 64 channels.
- ASAD board costs 200K JPY (3M KRW). It has 4 AGET chips or 256 channels on a board. For 10K channels, 40 ASADs are needed (120 M KRW)
- 10 CoBo boards /10K channel are needed. Each costs 400K JPY (6M KRW)

Cost estimates for the GET system (2)

- 1 Mutant card /10K channel is needed. The card costs 1M JPY (15M KRW).
- 1 μTCA crate /10K channel is needed. The crate costs 1.6M JPY (24M KRW).

- For 10K channel, the total cost would be 300M (AGET batch) + 120M (40 AsAds) + 60M (10 CoBos) + 15M (Mutant) + 24M (μTCA) = 520M = 0.5 B KRW

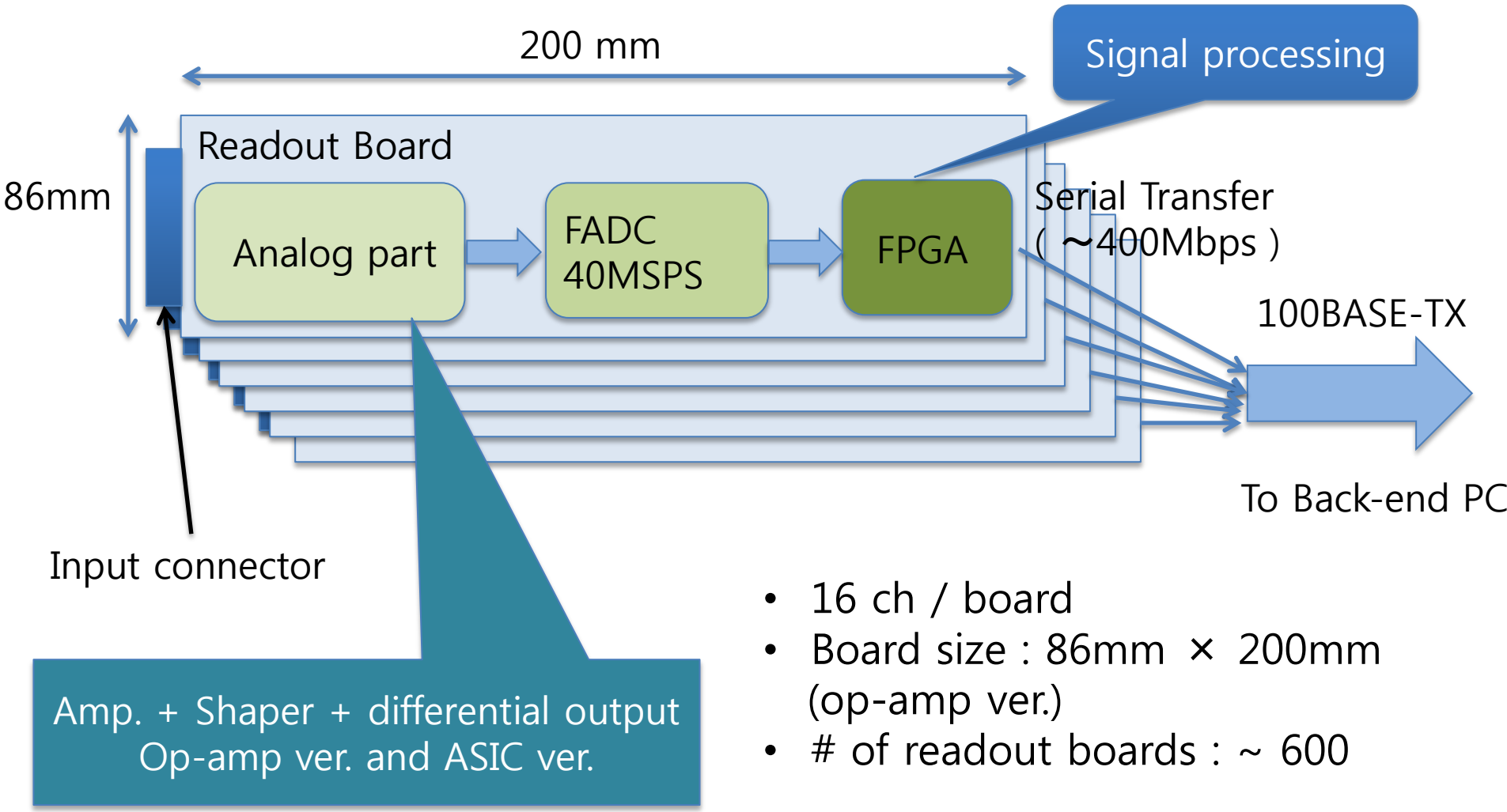
E42 with GETs

- Two AsAd v2.0 (pre-production) boards (w/ option for AGET-II chip replacement) at 4000 Euro/board (7.5M Won/board)
- AGET-I in Jan and AsAd boards in March, 2013
- FPGA Xilinx development kit (ML507).
- Full version available in August, 2013.

LEPS2 TPC Electronics

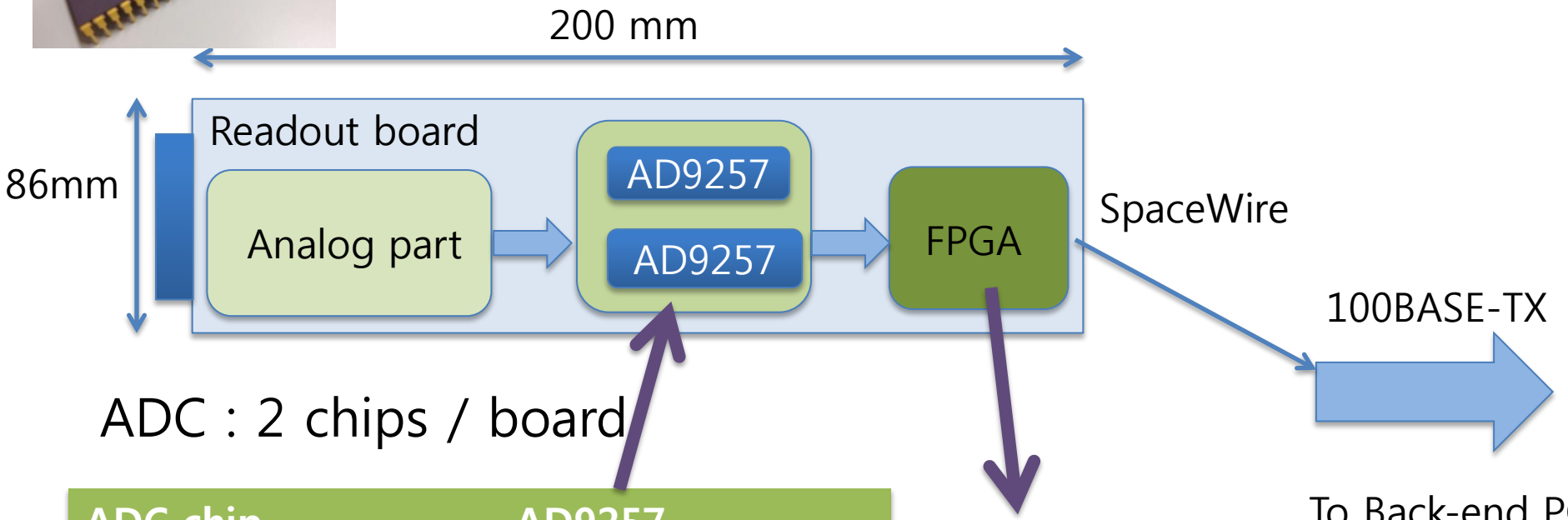
- Analog part : ASIC for lowering power consumption. Op-amp backup version.
- Power consumption : ASIC ver. : 710W, Op-amp ver. : 1kW
- Event rate is 5-10 kHz.
- Prototype ASIC chips available now. Mass production is expected in March, 2013.
- 10,000 ch readout boards by 2014.

LEPS2 TPC Readout Board



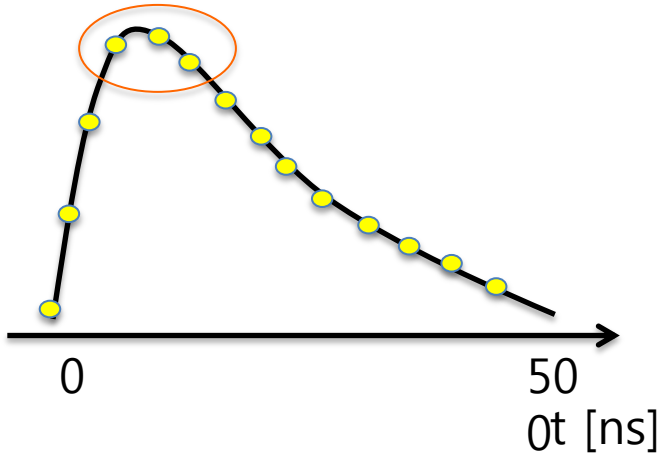
- 16 ch / board
- Board size : 86mm × 200mm (op-amp ver.)
- # of readout boards : ~ 600

ADC



ADC : 2 chips / board

ADC chip	AD9257
# of channels	8 ch
ENOB	14 bit
Sampling rate	40 MSPS
Output	Serial LVDS
Operating voltage	1.8 V
Power consumption	55 mW /ch



Our Strategy

- Collaboration with GET group and LEPS2 group.
- Test GET and LEPS2 prototypes, and contribute to TPC electronics in an experiment (Samurai or J-PARC-E42) with GET and the LEPS2.
- Develop our own electronics for LAMPS-TPC (a long-term project : TDC-based electronics).